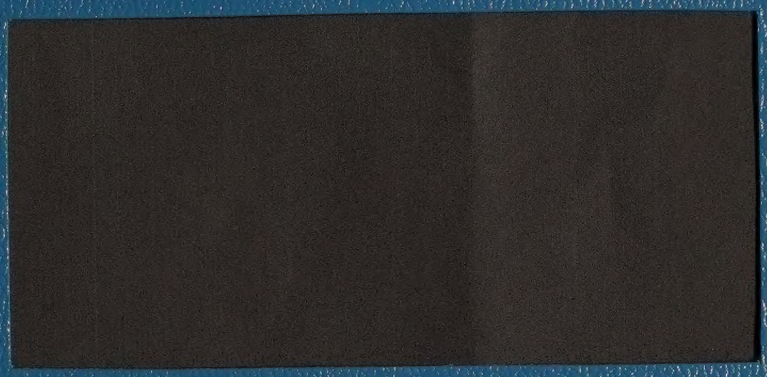
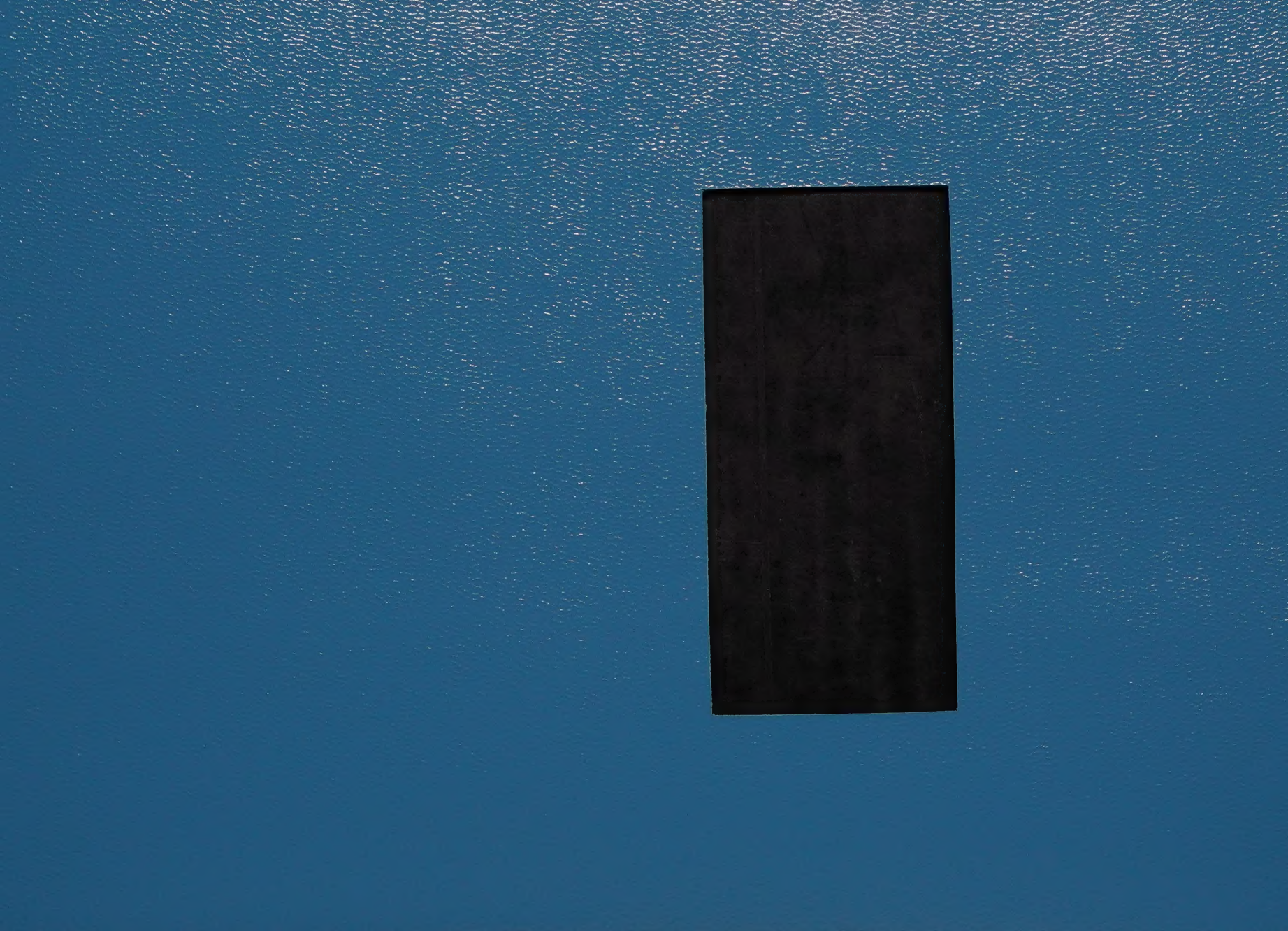


ITHACO



MICROFICHED

ITHACO Model 488A & 488A-2

GPIB Coupler

Instruction Manual

August 1983

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APPENDIX A ICS Electronics Corporation IEEE-488 Bus Interface Card

SECTION 1

INTRODUCTION

The ITHACO Model 488 Coupler is a device that takes status and control lines from selected ITHACO data acquisition equipment via a back panel connector and converts these lines to an IEE-488 format bus which can be directly connected to any computer having and IEE-488 port. The coupler is internally programmed by a prom to enable the computer to communicate with the desired ITHACO instrument. The Model 488A Coupler is programmed for connection with ITHACO Model 1201-06 Preamplifiers or ITHACO Model 397EO-05-06 Lock-In Amplifiers. The choice is made by a switch selection inside the coupler. The Model 488A-2 Coupler contains a different prom which allows the coupler to interface with ITHACO Model 450 series M27 Amplifiers.

SECTION 2

INSTALLATION

2.1 INSPECTION

2.1.1 General

Before shipment, this unit was found to be free of electrical and mechanical defects. As soon as the instrument is unpacked, inspect for any damage that may have occured in transit. Save all packing materials until the inspection is complete. If damaged in any way, a claim should be filed with the carrier and a copy forwarded to ITHACO. ITHACO will then advise you as to the disposition of the equipment and will arrange for repair or replacement without waiting for a claim against the carrier.

2.1.2 Visual Inspection

A visual check should be made to confirm that there are no broken knobs or connectors, and that the case and panel surfaces are free of dents and scratches.

2.1.3 Electrical Inspection

The instrument should be checked against its electrical specifications.

2.2 POWER REQUIREMENTS

Before applying power to the 488A or 488A-2 coupler, check to be certain that the instrument is set properly for the AC line voltage. A rear panel switch allows selection of 115V AC or 230V AC (50-60 Hz) line operation. Also check to be certain that the power fuse is installed:

115V AC operation - .5A Fuse

230V AC operation - .25A fuse

2.2.1 Program Selection for the 488A Coupler (1201 - 397 SERIES)

The program selection switches are located near the center of the 488A printed circuit board. To access these switches, it is necessary to remove the top cover from the coupler. First, remove the power cord and all other rear panel connections. Next, remove

the four screws which secure the cover on the bottom of the unit. Finally, slide the cover assembly to the rear of the coupler.

To select the 1201-06 program, slide all four switches to the off position. To select the 397EO-05-06 program, slide switch 1 to the on position. Switches 2, 3 and 4 should remain in the off position. (see Fig. 3.1)

Replace the top cover.

2.2.2 Program Selection for the 488A-2 Coupler (450 Series)

The 488A-2 coupler is programmed for operation with ITHACO Model 450 series Amplifiers only and program switch selection is not necessary. All program switches should be in the "off" position. The physical location of this switch group is described above in paragraph 2.2.1.

2.3 ADDRESS SWITCH

The 488A copuler may be set to Talk/Listen addresses 0-30 by setting the Address Switch on the rear panel. The binary weight of switch elements are as follows:

Position	Binary Weight
5	2^4
4	2^3
3	2^2
2	2^1
1	2^0
T	-
L	-

For example, address 8 would be selected by turning on switch number 4 ($2^3 = 8$) as illustrated in Figure 3.2.

For normal operation (addressing by the computer) the 'talk only' and 'listen only' switches (T & L) must be in the off position.

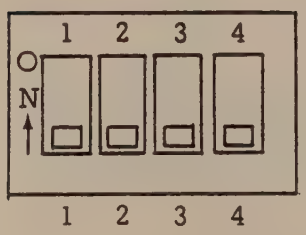
2.4 INTERCONNECTION

Using the appropriate cable and coupler, connect the coupler to either the 450M27 Rack, 1201-06 or 397EO-05-06. Be certain that the connectors are mated securely. Connection to the IEEE 488 Bus is via a standard connector on the rear panel of the coupler. Do not attempt to connect the 1201, 450M27 or 397 directly to the Bus.

	INSTRUMENT MODEL #	COUPLER MODEL #	CABLE MODEL #
	(1 TO 7) 450 SERIES M27 AMPLIFIERS WITH APPROPRIATE M27 EQUIPMENT RACK	488A-2	450V4
	397EO-05-06	488A	397V1
1	1201-06	488A	1201V1
2	1201-06	488A	1201V2, 1201V5
3	1201-06	488A	1201V3, 1201V5 1201V6
4	1201-06	488A	1201V4, 1201V5 1201V6, 1201V7

Program Select Switch (on PC Board)

Fig. 2.1



	1201	397	450(488A-2 Coupler)
1	0	1	0
2	0	0	0
3	0	0	0
4	0	0	0

Address Switch (Rear Panel)

Fig. 2.2 Shown in address "8" position.

SECTION 3

488A OPERATION

The operation of the ITHACO Model 488A GPIB Coupler with the Model 1201-06 Preamplifier and 397EO-05-06 Lock-in Amplifier is described in this section. Before proceeding, check to be certain that all installation requirements of Section 2 have been met.

Status of the coupler is indicated by four front panel lights: Power, Ready, My Talk Address (MTA) and My Listen Address (MLA). The MTA and MLA lamps come on when the coupler is addressed as a talker or listener, respectively.

Three front panel pushbutton switches are provided for power on/off, reset and SRQ inhibit. The coupler is equipped with a power on reset function. However, if the couplers address or program selection switch is changed after power on, the reset button must be momentarily depressed to load the new setting. The SRQ inhibit switch prevents all SRQ signals generated by the interface from reaching the bus. The reset button must be momentarily depressed each time the postion of this switch is changed.

3.1 PROGRAMMING THE 1201-06 PREAMPLIFIER VIA THE BUS

All programming functions available on the 1201-06 RPO have been implemented with the 488A coupler. A detailed discussion may be found in the 1201 manual. For convenience, they are summarized below.

Gain — The gain of the 1201 can be programmed remotely via the bus when the front panel gain switch is in the "R" position. If the gain switch is in any other position, the switch selected gain can be read by the controller.

High Pass Filter — The status of high pass filter switch may be read when the coupler is addressed as a Talker, provided the corresponding select code was sent during the previous Liston command. The high pass filter setting cannot be programmed via the bus.

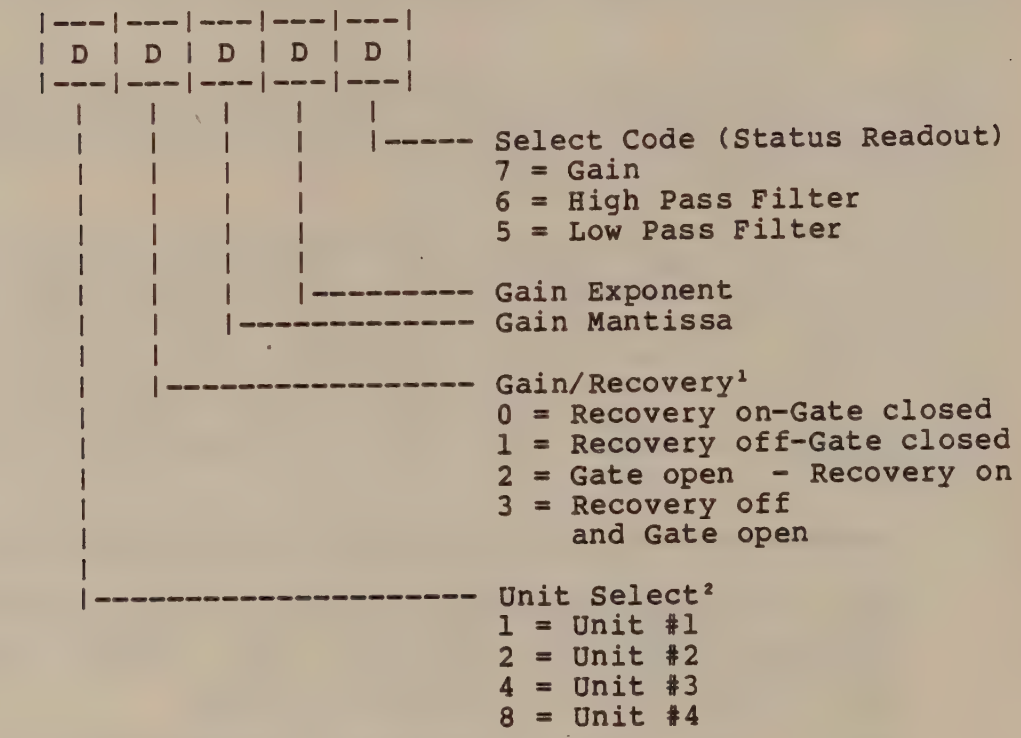
Low Pass Filter — The status of the low pass filter switch may be read when the coupler is addressed as a Talker, provided the corresponding select code was sent during the previous Listen command. The low pass filter setting cannot be programmed via the bus.

Gate — The signal path gate may be operated either by the rear panel BNC connector or by the bus.

Other Functions Overload recovery may be activated as a Listen function. Overload is indicated as a Talk function.

3.1.1 Listen Format

The following 5 digit code is used to program the 1201-06 from the controller.



Example

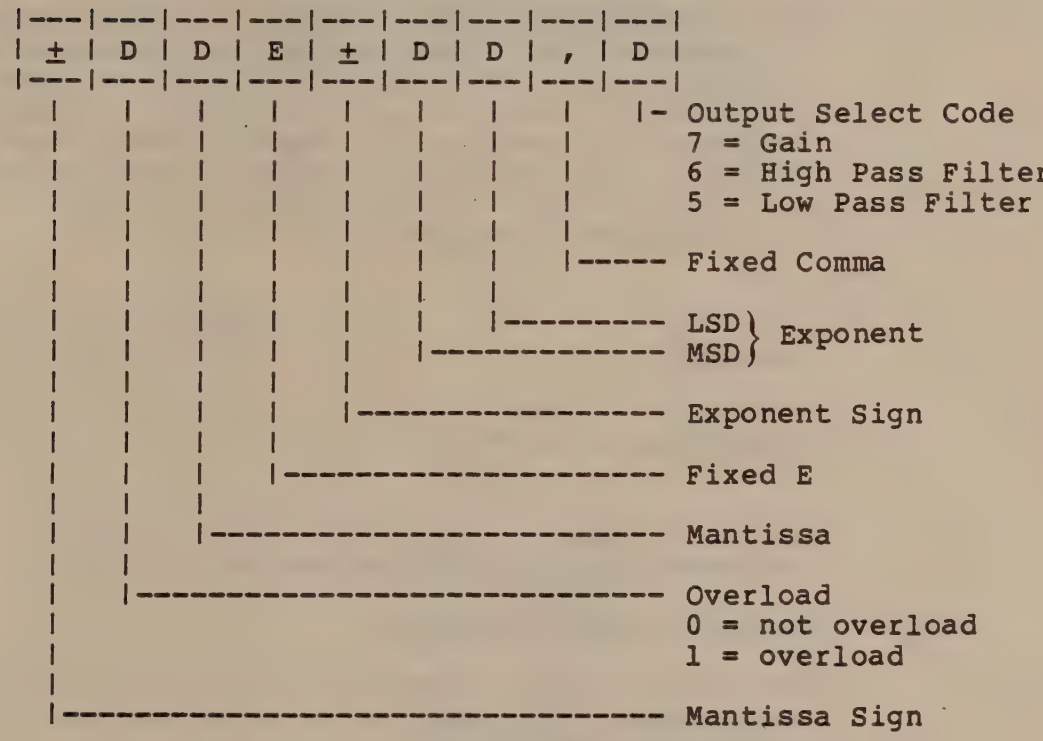
1 3 5 2 6	Unit #1 is selected Recovery is off & Gate is open Gain Sent is 500 The High Pass Filter setting be returned on the next "Talk" cycle.

The Gate/Recovery digit is structured as follows:

bit 0 $\overline{\text{RECY}}$ (Pin 30 on 1201-06)
bit 1 GATE (Pin 32 on 1201-06)
bit 2 ----
bit 3 ----

3.1.2 Talk Format

The status of the 1201-06 may be determined from the following code returned when the 488A copuler is addressed as a Talker.



Examples

+ 03 E - 01, 6 ---- High Pass Filter Setting .03

+ 15 E + 02, 7 ---- Gain Setting 500, overload

+ 03 E + 04, 5 ---- Low Pass Filter Setting 300K

3.1.3 Data Transfer Between Preamp and Bus Coupler

New data is strobed into the couplers data latch each time the coupler is addressed as a Talker or Listener. In order to avoid timing errors, data is strobed in before the Listen code is outputted to the 1201. It is possible, therefore, that the code returned to the controller on a Talk command does not indicate the current status of the 1201. To avoid

this potential error, it is recommended that two Talk commands be implemented each time data is requested from the 1201. The first Talk command updates the 488A data latch. The second Talk command transmits the updated information over the bus.

3.1.4 SRQ

The GPIB SRQ (service request) function has been implemented for overload and gain vernier on. This function may be disabled by use of the front panel SRQ inhibit switch as described in Section 3.0. Relmember to momentarily depress the reset button each time the SRQ inhibit switch position is changed.

3.1.5 SRQ Response Characters

SRQ Condition	Response Character Bits 8	7	6	5	4	3	2	1
OVERLOAD	0	1	0	0	0	0	1	0
GAIN VERNIER ON	0	1	0	0	0	1	0	0

Bit #7 is used by the 488A to indicate a service requesst condition to the bus controller.

3.1.6 Initial Status on Reset

The 488A coupler is set in a defined initial state when power is turned on or when the reset button is momentarily depressed.

Gain:	10
Select Code:	7 (gain)
Gate:	closed
Recovery:	off

3.2 PROGRAMMING THE 397EO-05-06 LOCK-IN AMPLIFIER VIA THE BUS

All programming functions available on the 397EO-05-06 have been implemented with the 488A coupler. A detailed discussion may be found in the 397EO manual. For convenience, they are summarized below.

Gain The sensitivity of the 397EO-05-06 can be programmed remotely via the bus when the front panel sensitivity switch is in the "R" position.

Expand 10 X The 10 X expand function may be controlled via the bus. If the lock-in is in the 10 X expand mode, the coupler will return an exponent of 10 in the

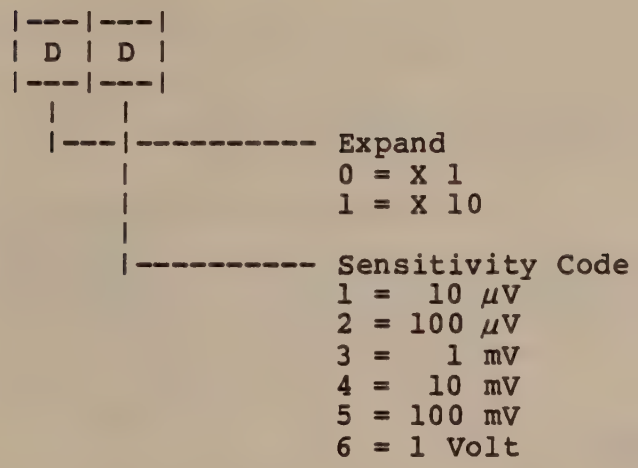
output code.

No Lock/Overload A "no lock" or "overload" condition is indicated by the output code when the 488A is addressed as a talker. These conditions also generate an SRQ.

Output The BCD output of the 397EO-05-06 is fed to the bus when the 488A is addressed as a talker.

3.2.1 Listen Format

The following two digit code is used to program the 397EO-05-06-07 from the controller.

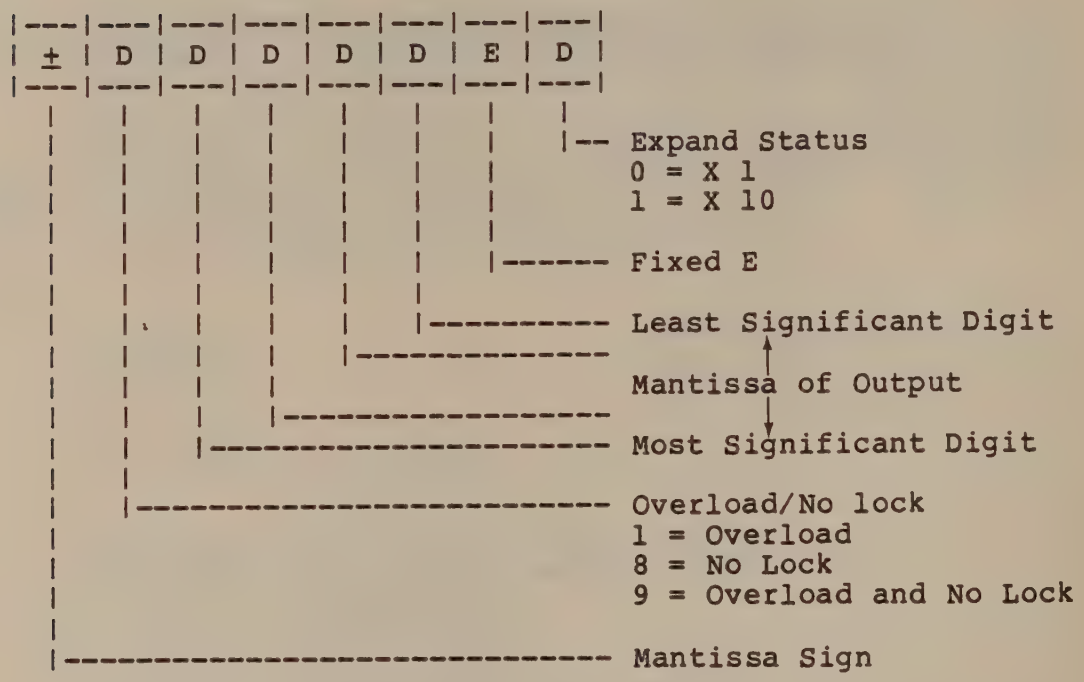


Examples:

Code	Full Scale Sensitivity
01	10 μV
11	1 μV
05	100 mV
16	100 mV

3.2.2 Talk Format

The status and output of the 397EO-05-06 is transmitted via the bus when the 488A coupler is addressed as a talker. The format of the code is as follows:



Examples

+ 0 1 1 2 5 E 1 ---- Output is 1.125 X 10 X full

+ 8 X X X X E 0 ---- Reference unlock, expand not on, mantissa is not valid (X = any number).

3.2.3 Data Transfer Between Lock-in Amplifier and Bus Controller

Data is transferred to the couplers I/O latch when the data valid line (pin 4) of the 397EO-05-06 is high. Data is not updated until the latched data is moved onto the bus when the coupler is addressed as a talker. It is recommended, therfore, that if the coupler is addressed as a talker on a cycle time significantly longer than the conversion time of the BCD option in the lock-in amplifier, then two talk commands should be issued for each reading. The first talk command is used to update the data latch. The second talk command transmits updated information over the Bus.

3.2.4 SRQ

The GPIB SRQ (service request) function has been implemented for overload and no lock conditions. This function may be disabled by use of the front panel SRQ inhibit switch as described in Section 3.0. Remeber to momentarily depress the reset button each time the SRQ inhibit switch position is changed.

3.2.5 SRQ Response Characters

Condition Generating SRQ	Response Character Bits 8	7	6	5	4	3	2	1
OVERLOAD	0	1	0	0	0	0	1	0
NOLOCK	0	1	0	0	0	1	0	0

Bit #7 is used by the 488A to indicate a service request condition to the Bus Controller.

3.2.6 Initial Status on Reset

The 488A coupler is set in a defined initial state when power is turned on or when the reset button is momentarily depressed.

Gain: 0
Expand: X 1

SECTION 4

488A-2 OPERATION

4.1 PROGRAMMING THE 450M27 AMPLIFIERS VIA BUS

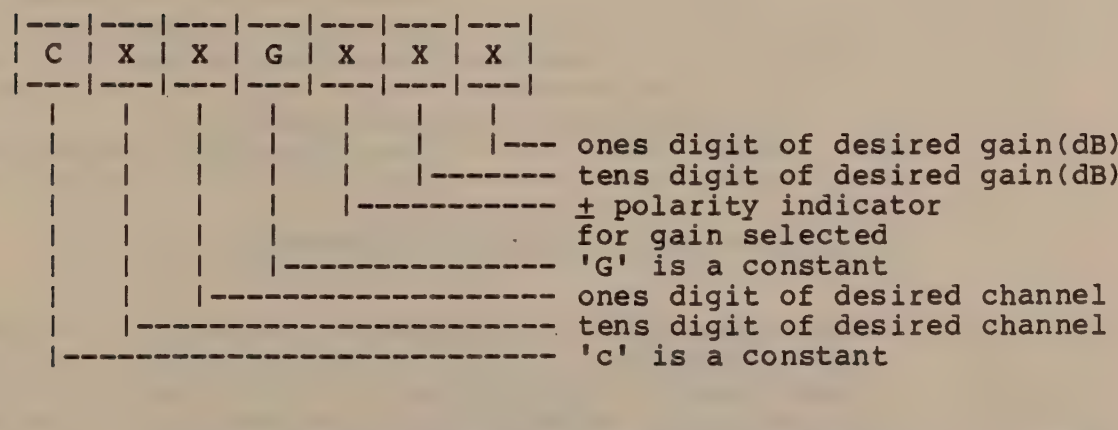
Programming of up to 2 racks (14 amplifier channels) can be individually implemented with the 488A-2 copuler as described below:

Gain — The gain of the 450M27 can be programmed remotely via the bus when the front panel gain switch is in the remote ("R") position. If the gain switch is in any other position, the switch selected gain can only be read by the controller.

Rolloff — If a switchable Rolloff selector is included on your model 450M27, the rolloff may be read along with the gain status by the controller. The rolloff however, cannot be remotely commanded by the controller.

4.1.1 List Format

When computer controlling the 450 OPT 27 amplifiers, via the 488A-2 coupler, a channel may be selected and its gain set by printing the following 7 digit code from the controller.


C X X G X X X
ones digit of desired gain(dB)
tens digit of desired gain(dB)
± polarity indicator for gain selected
'G' is a constant
ones digit of desired channel
tens digit of desired channel
'c' is a constant

Note: The 450 Option 27 amplfiers must be in remote to receive gain control commands from the controller.

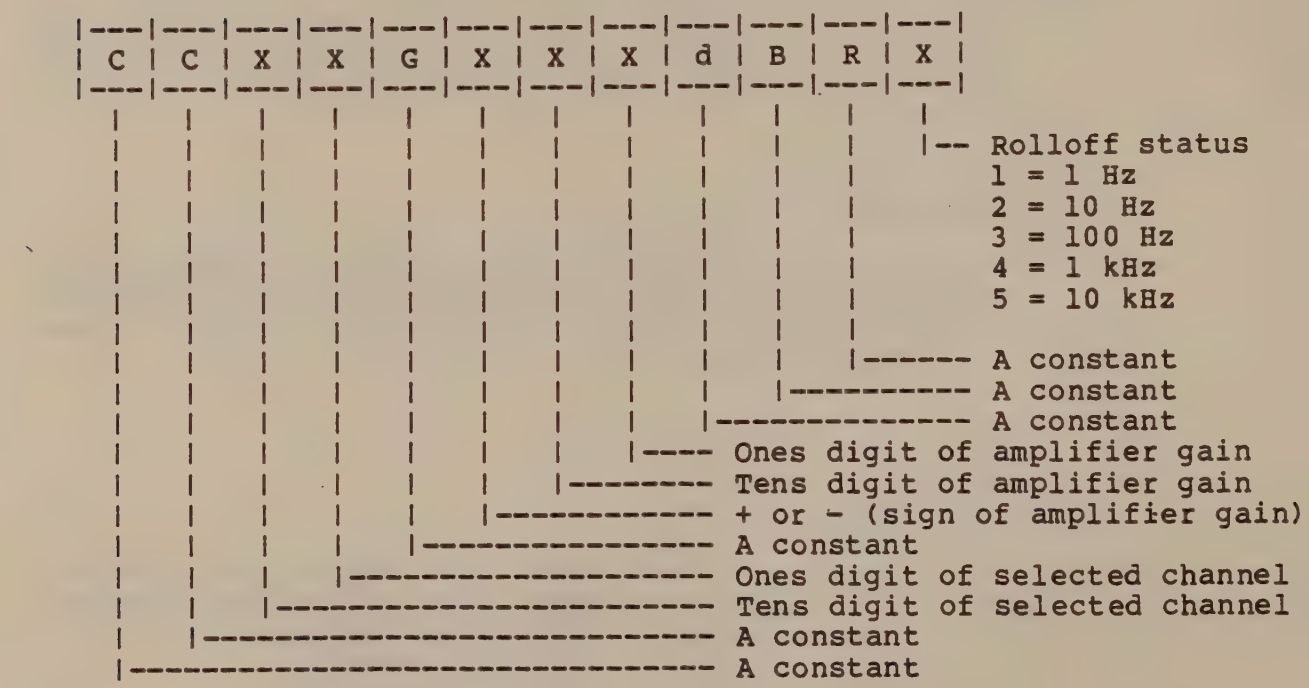
Example

| C | 0 | 2 | G | + | 0 | 5 | Channel #2 is selected and gain is set to +5 dB.

| C | 1 | 1 | G | - | 1 | 0 | Channel #11 (rack #2 channel #4) is selected and gain is set to -10 dB.

4.1.2 Talk Format

When computer controlling the 450 Opt 27 amplifiers via the 488A-2 coupler, a channel may be selected and its gain and rolloff status read by the controller, when the controller inputs the following code:


C C X X G X X X d B R X
Rolloff status
1 = 1 Hz
2 = 10 Hz
3 = 100 Hz
4 = 1 kHz
5 = 10 kHz
A constant
A constant
A constant
Ones digit of amplifier gain
Tens digit of amplifier gain
+ or - (sign of amplifier gain)
A constant
Ones digit of selected channel
Tens digit of selected channel
A constant
A constant

This code is always of the last amplifier commanded (as in Section 4.1.1). If the amplifiers are in the remote mode the controller usually is set up to input the read code immediately following the printed write command. If the amplifiers are not in remote, the amplifiers will not accept a printed write command but will read back the actual manual gain setting of the amplifier commanded after your controller input statement.

Example (Remote Mode)

If the controller prints a comand of

C	0	1	G	+	1	0

and the controller then inputs a code from the amplifier. The code will read

C	C	0	1	G	+	1	0	D	B	R	2

this signifies that the channel #1 gain status is +10dB with 10Hz rolloff.

Example (Local Mode)

The controller prints a command to the amplifier whose gain and rolloff status is wanted:

C	0	2

the controller then inputs a code from the amplifier The code would read

C	C	0	2	G	+	3	5	D	B	R	1

indicating channel #2 gain status is +35dB with a 1 Hz rolloff.

4.1.3 Data Transfer Between the 450 M27 and the 488A-2 Bus Coupler

New data is strobed into the 488A-2 data latches each time the coupler is addressed as a talker or listener. To avoid timing errors, data is strobed in before the listen code is outputed to the 450M27. It is possible therefore that the code returned to the controller does not indicate the current status of the 450M27. To avoid this potential error, it is recommended that 2 talk commands be made each time data is requested from the 450M27. The first command is used to update the 488A-2 data latches and the second talk command transmits the updated information over the bus.

4.1.4 SRQ

The GPIB SRQ (service request) function is not used with the 450M27 amplifier.

4.1.5 450M27 Status Format

The following tables give the status codes for a 450M27 and are included for academic and for troubleshooting aids.

WRITE MODE

The 450 Gain switch must be in the Remote position for writing Gain Status to the amplifier.

Set the Read/$\overline{\text{Write}}$ line (P1–16) to logic 0

Set Command $\overline{\text{Strobe}}$ line (P1–8) to logic 0 to transfer the data written on gain status lines.

1 = +5V, 0 = Logic Ground, X = 0 or 1

Gain Status Lines					Amplifier Gain
$\overline{8}$	$\overline{4}$	$\overline{2}$	$\overline{1}$	5 dB	dB
1	1	1	1	1	–10
1	1	1	0	1	0
1	1	0	1	1	10
1	1	0	0	1	20
1	0	1	1	1	30
1	0	1	0	1	40
1	0	0	1	1	50
1	0	0	0	1	60
0	1	1	1	1	70
0	1	1	0	1	80
X	X	X	X	0	To add +5 dB on to desired gain setting

Written data is latched until the next transition from +5V to 0 on the Command $\overline{\text{Strobe}}$ line. Then whatever information that is on the gain status lines is loaded into the data latches.

READ MODE

0 = GND, 1 = +5V, X = 0 or 1

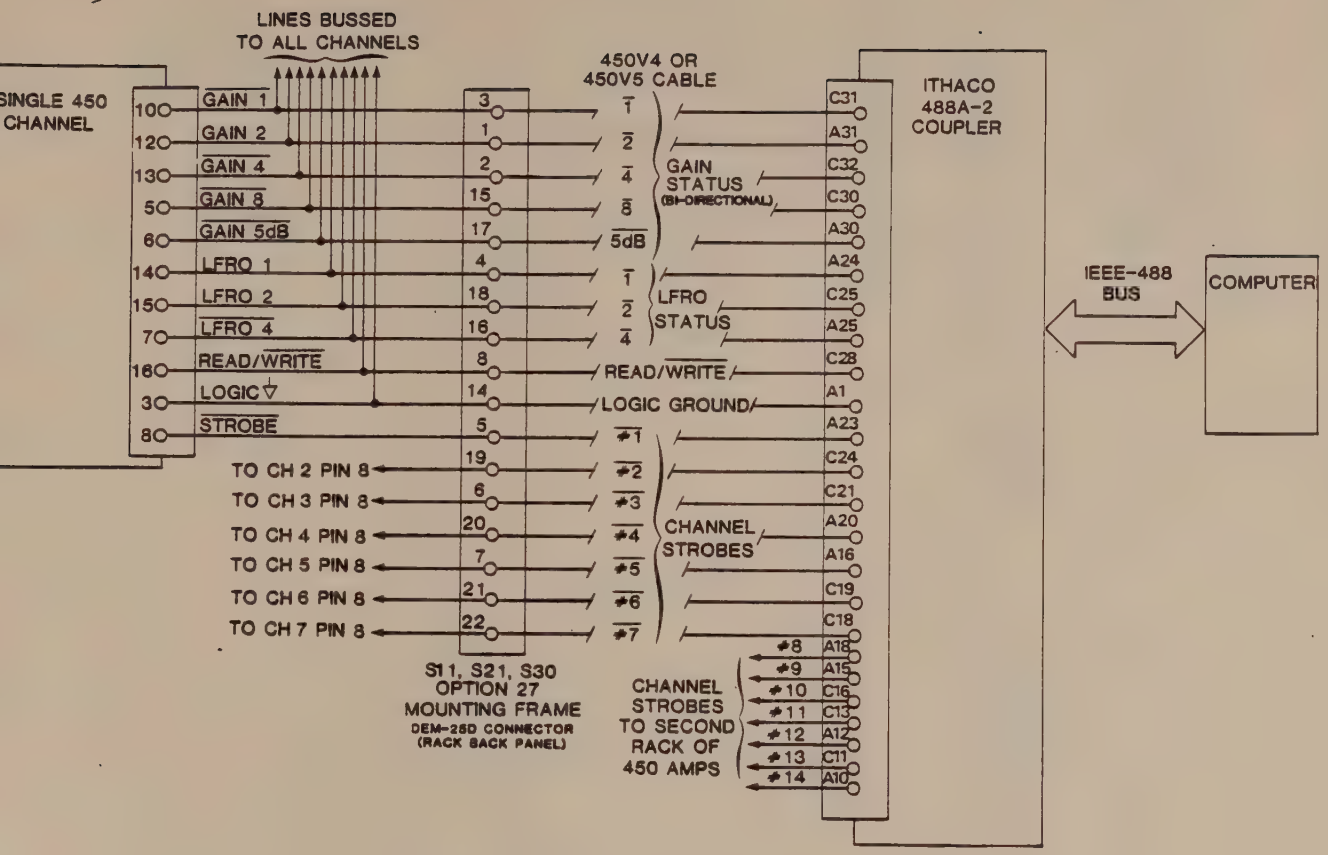
READ/$\overline{\text{WRITE}}$ LINE P1#16 = 1 (+5V)

COMMAND $\overline{\text{STROBE}}$ LINE P1#8 = 0 (GND)

Amplifier Gain	Gain Status Lines				
dB	$\overline{8}$	$\overline{4}$	$\overline{2}$	$\overline{1}$	$\overline{5}$ dB
–10	1	1	1	1	1
0	1	1	1	0	1
10	1	1	0	1	1
20	1	1	0	0	1
30	1	0	1	1	1
40	1	0	1	0	1
50	1	0	0	1	1
60	1	0	0	0	1
70	0	1	1	1	1
80	0	1	1	0	1
Selected Gain +5 dB	X	X	X	X	0

Amplifier Rolloff	Rolloff Status Lines		
Hz	$\overline{4}$	$\overline{2}$	$\overline{1}$
1	1	1	1
10	1	1	0
100	1	0	1
1K	1	0	0
10K	0	1	1

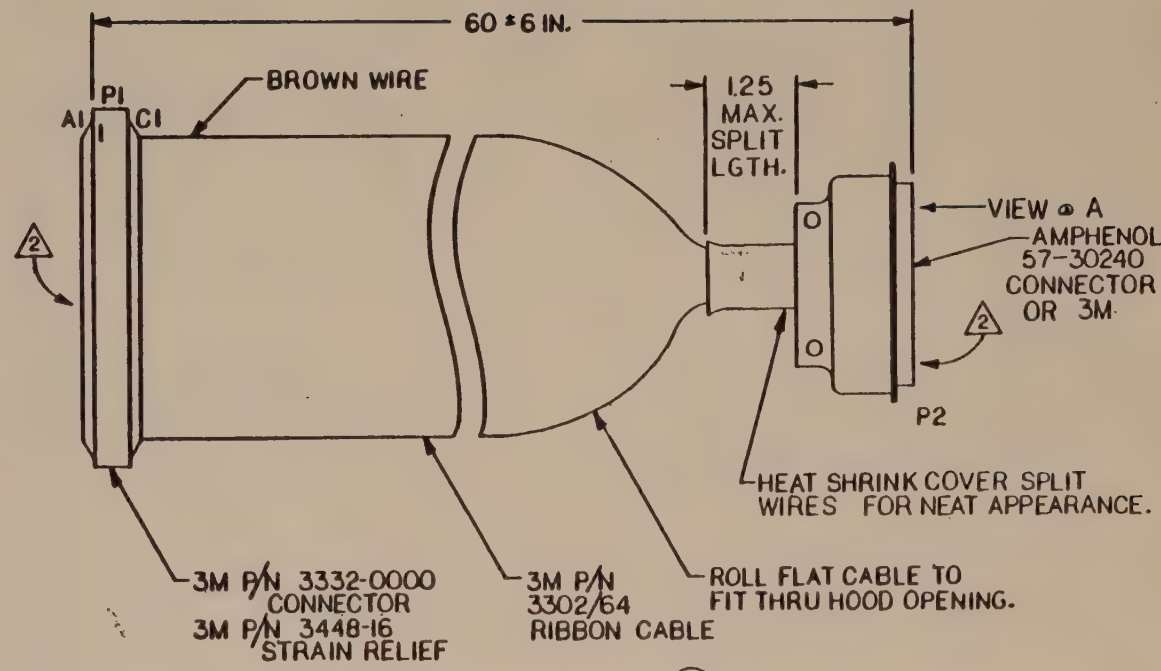
Gain and Rolloff Status can be read while the amplifier is in the local or remote position.


LINES BUSSED
TO ALL CHANNELS
SINGLE 450
CHANNEL
GAIN 1
GAIN 2
GAIN 4
GAIN 8
GAIN 5dB
LFRO 1
LFRO 2
LFRO 4
READ/WRITE
LOGIC
STROBE
TO CH 2 PIN 8
TO CH 3 PIN 8
TO CH 4 PIN 8
TO CH 5 PIN 8
TO CH 6 PIN 8
TO CH 7 PIN 8
S11, S21, S30
OPTION 27
MOUNTING FRAME
DEM-25D CONNECTOR
(RACK BACK PANEL)
450V4 OR
450V5 CABLE
GAIN
STATUS
(BI-DIRECTIONAL)
LFRO
STATUS
READ/WRITE
LOGIC GROUND
CHANNEL
STROBES
CHANNEL
STROBES
TO SECOND
RACK OF
450 AMPS
ITHACO
488A-2
COUPLER
IEEE-488
BUS
COMPUTER

CH 1	A 30	19	EXP. CTL	
CH 2	C 31	—		
CH 3	A 31	—		
CH 4	C 32			
CH 5	C 30	22	GA	
CH 6	A 29	21	GB	
CH 7	C 29	20	GC	
CH 8	A 28	—		
CH 9	C 28			
CH 10	A 27			
CH 11	C 27			
CH 12	A 26			
CH 13	A 24			
CH 14	C 25			
CH 15	A 25			
CH 16	C 26			
CH 17	A 22			
CH 18	C 23			
CH 19	A 23			
CH 20	C 24			
CH 21	C 22	—		
CH 22	A 21	3*	OVLD	SRQ
CH 23	C 21	2*	NO LOCK	
CH 24	A 20	—		
CH 25	C 20	5	SIGN	±
CH 26	A 19	—		
CH 27	A 16	—		
CH 28	C 19	—		
CH 29	C 17	3*	OVLD	
CH 30	A 17			OVER
CH 31	C 18	—		
CH 32	A 18	2*	NO LOCK	
CH 33	A 14	6	100	MSD
CH 34	C 15		200	
CH 35	A 15		400	
CH 36	C 16		800	
CH 37	C 14	10	10	MSD-1
CH 38	A 13	9	20	
CH 39	C 13	8	40	
CH 40	A 12	7	80	
CH 41	C 12	14	1	MSD-2
CH 42	A 11	13	2	
CH 43	C 11	12	4	
CH 44	A 10	11	8	
CH 45	A 8	18	.1	LSD
CH 46	C 9	17	.2	
CH 47	A 9	16	.4	
CH 48	C 10	15	.8	
CH 49	A 6	1	EXP STS	EXP
CH 50	C 7	—		
CH 51	A 7	—		
CH 52	C 8	—		
EDRI	A 2	4	DATA VALID	
INHI	C 2	—		
STAT A	C 6	23	REM STS	
STAT B	A 5			
REM	C 4			
CLR	A 4			
DATA I	C 5			
TRG	C 1			
+5v	A 32			
GND	A 1	24	DIG GND	

SEE NOTE (2)

VIEW A



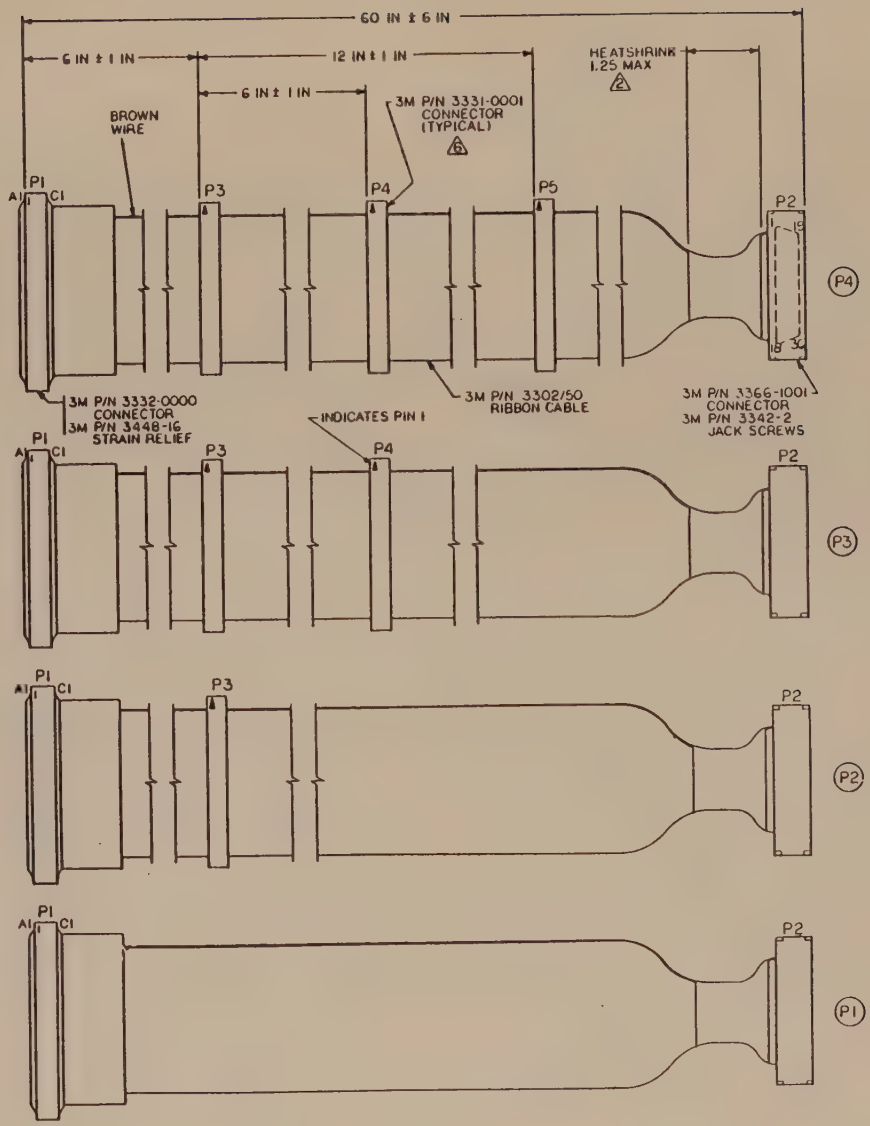
(P1)

NOTE:
1.* INDICATES 2 WIRES IN SAME CONNECTOR PIN.
(2) ALL WIRE CONNECTIONS SHOWN IN WIRING DIAGRAM TO BE MADE IN P2.

ITH DWG C88724 REV C 10/81

MODEL 397V1 INTERFACE CABLE – ASSEMBLY

SIGNAL FUNC	P1 PIN #	WIRING DIAGRAM 2	P2 PIN #	WIRE COLOR	P3,P4 P5 PIN #	1201 FUNCTION	
CH1	A 30		34	5-GRN	45	DSEL #1	
CH2	C 31		—	5-GRY	48	DSEL #2	
CH3	A 31		—	5-VIO	47	DSEL #3	
CH4	C 32		—	5-BLK	50	DSEL #4	
CH5	C 30		30	5-BLU	46	$\overline{RECY}$	
CH6	A 29		32	5-YEL	44	$\overline{GATE}$	
CH7	C 29		—	—	—	—	
CH8	A 28		—	—	—	—	
CH9	C 28		20	5-ORN	43	GA	
CH10	A 27		21	5-BRN	41	GB	
CH11	C 27		22	5-RED	42	GC	
CH12	A 26		—	—	—	—	
CH13	A 24		23	4-VIO	37	EXP A	
CH14	C 25		24	4-WHT	39	EXP B	
CH15	A 25		25	4-GRY	38	EXP C	
CH16	C 26		26	4-BLK	40	EXP D	
CH17	A 22		27	4-ORN	33	SEL 1	
CH18	C 23		28	4-BLU	36	SEL 2	
CH19	A 23		29	4-GRN	35	SEL 3	
CH20	C 24		—	—	—	—	
CH21	C 22		—	4-YEL	34	—	
CH22	A 21		17 *	4-BRN	31	OVLD	SRQ
CH23	C 21		6	4-RED	32	MLT	
CH24	A 20		—	3-WHT	29	—	
CH25	C 20		7	3-BLK	30	MS	±
CH26	A 19		—	3-VIO	27	—	
CH27	A 16		—	3-BRN	21	—	
CH28	C 19		—	3-GRY	28	—	
CH29	C 17		17 *	3-YEL	24	OVLD	OVLD
CH30	A 17		—	3-ORN	23	—	
CH31	C 18		—	3-BLU	26	—	
CH32	A 18		—	3-GRN	25	—	
CH33	A 14		2	2-VIO	17	MA	
CH34	C 15		3	2-BLK	20	MB	MSD
CH35	A 15		4	2-WHT	19	MC	
CH36	C 16		5	3-RED	22	MD	
CH37	C 14		16	2-GRY	18	ES	±
CH38	A 13		—	2-GRN	15	—	
CH39	C 13		—	2-BLU	16	—	
CH40	A 12		—	2-ORN	13	—	
CH41	C 12		15	2-YEL	14	EE	EXP
CH42	A 11		—	2-BRN	11	—	
CH43	C 11		—	2-RED	12	—	
CH44	A 10		—	1-WHT	9	—	
CH45	A 8		11	1-BLU	6	EA	EXP
CH46	C 9		12	1-GRY	8	EB	
CH47	A 9		13	1-VIO	7	EC	
CH48	C 10		14	1-BLK	10	ED	
CH49	A 6		—	—	—	—	
CH50	C 7		—	—	—	—	
CH51	A 7		—	—	—	—	
CH52	C 8		—	—	—	—	
EDRI	A 2		—	1-RED	2	—	
INHI	C 2		—	—	—	—	
STAT A	C 6		10	1-GRN	5	REM	
STAT B	A 5		—	—	—	—	
REM	C 4		31	1-ORN	3	$\overline{GOR}$	
CLR	A 4		—	—	—	—	
DATA I	C 5		—	1-YEL	4	—	
TRG	C 1		—	—	—	—	
+5V	A 32		—	5-WHT	49	—	
GND	A 1		9	1-BRN	1	GND	
			1	—	—	VOUT	
			35	—	—	GCE 1	
			36	—	—	GCE 2	



P1 1201 V1
P2 1201 V2
P3 1201 V3
P4 1201 V4

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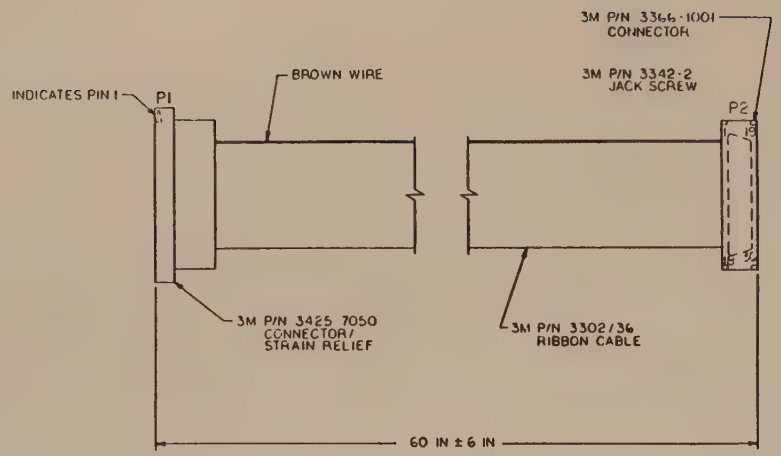
MODELS 1201V1 – 1201V4 INTERFACE CABLE – ASSEMBLY

P2 PIN #	WIRE COLOR	P1 PIN #	1201 FUNCTION
1	1-BRN	—	VOUT
19	1-RED	—	—
2	1-ORN	17	MA
20	1-YEL	43	GA
3	1-GRN	20	MB MSD
21	1-BLU	41	GE
4	1-VIO	19	MC MSD
22	1-GRY	42	GC
5	1-WHT	22	MD
23	1-BLK	37	EXP A
6	2-BRN	32	MLT
24	2 RED	39	EXP B
7	2-ORN	30	MS ±
25	2 YEL	38	EXP C
8	2-GRN	—	—
26	2 BLU	40	EXP D
9	2-VIO	1	GND
27	2 GRY	33	SEL 1
10	2 WHT	5	REM
28	2 BLK	36	SEL 2
11	3 BRN	6	EA EXP
29	3 RED	35	SEL 3
12	3 ORN	8	EB
30	3 YEL	46	RECY
13	3 GRN	7	EC
31	3 BLU	3	GOR
14	3 VIO	10	ED
32	3 GRY	44	GATE
15	3-WHT	14	EE EXP
33	3 BLK	—	—
16	4-BRN	18	ES ±
34	4 RED	●	●
17	4-ORN	24	OVLD OVLD
35	4-YEL	13	GCE 1
18	4-GRN	—	—
36	4-BLU	15	GCE 2
—	—	16	—
—	—	21	—
—	—	23	—
—	—	25	—
—	—	26	—
—	—	27	—
—	—	28	—
—	—	29	—
—	—	34	—
—	—	49	—



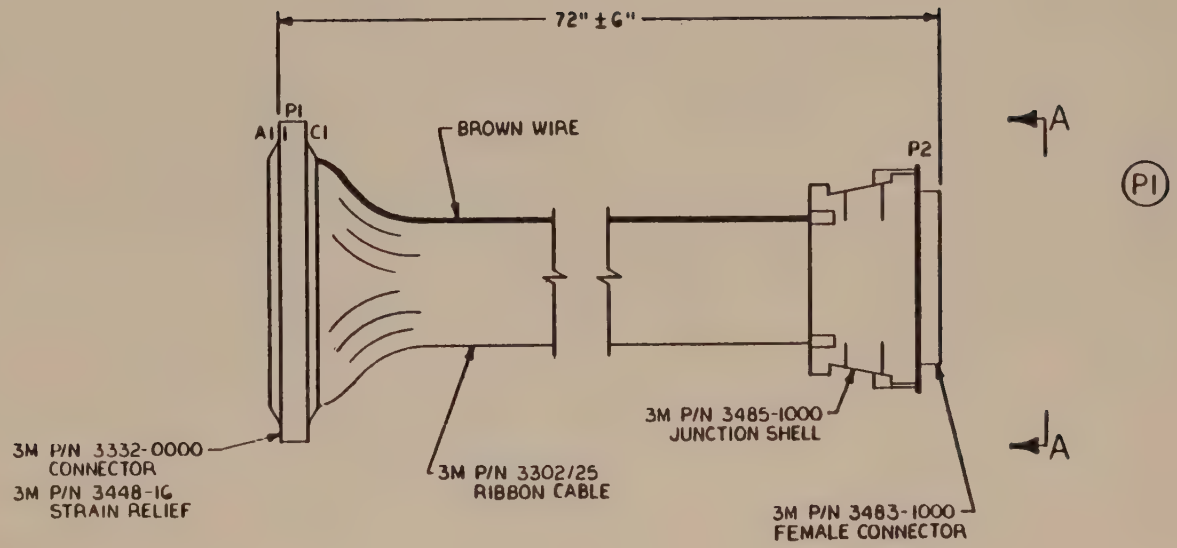
(P1) 1201 V5
(P2) 1201 V6
(P3) 1201 V7

●	P1 PIN #	1201 FUNCTION
PART 1:	48	DSEL #2
PART 2:	47	DSEL #3
PART 3:	50	DSEL #4

MODELS 1201V5 – 1201V7 INTERFACE CABLE – ASSEMBLY

P1	P2	DESCRIPTION
A30	17	$\overline{5}$ db
C31	3	$\overline{1}$ GAIN
A31	1	$\overline{2}$ GAIN
C32	2	$\overline{4}$ GAIN
C30	15	$\overline{8}$ GAIN
C28	8	READ/WRITE
A24	4	$\overline{1}$ ROLLOFF
C25	18	$\overline{2}$ ROLLOFF
A25	16	$\overline{4}$ ROLLOFF
A23	5	CHANNEL # 1 STROBE
C24	19	CHANNEL # 2 STROBE
C21	6	CHANNEL # 3 STROBE
A20	20	CHANNEL # 4 STROBE
A16	7	CHANNEL # 5 STROBE
C19	21	CHANNEL # 6 STROBE
C18	22	CHANNEL # 7 STROBE
A1	14	LOGIC GROUND

VIEW A-A



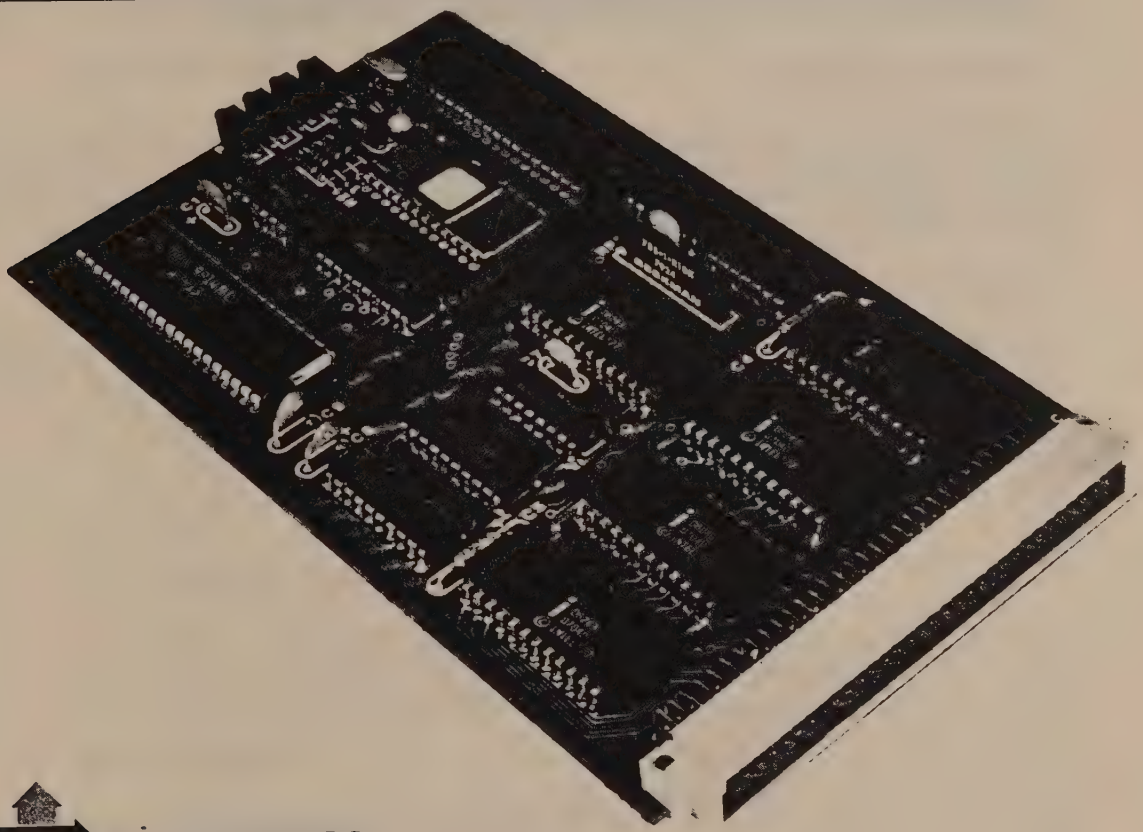
MODEL 450V4 INTERFACE CABLE – ASSEMBLY

APPENDIX A

ICS Electronics Corporation

IEEE-488 Bus Interface Card

MODEL 4823
IEEE 488 Bus Interface Card
Installation and Service Manual



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Publication Number 120008 Rev. 2
June 1982 Edition
(For program revisions 4.0 and up.)

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LIMITED OEM WARRANTY

Within 14 months of delivery, to an OEM purchaser, ICS Electronics Corporation will repair or replace at our option this ICS product if any part is found to be defective in materials or workmanship. Labor is included. Return this product to ICS Electronics or other designated repair station, freight prepaid, for prompt repair or replacement. Contact ICS for a return material authorization prior to returning the product for repair.

CERTIFICATION

ICS Electronics Corporation certifies that this instrument was carefully inspected and tested at the factory prior to shipment and was found to meet all requirements of the specification under which it was furnished.

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OEM PURCHASER

An OEM Purchaser is defined as anyone who purchases a 4823 Coupler Module with a customized PROM, from either ICS Electronics Corporation or from an authorized distributor, for resale as part of a larger device or system.

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1

Specifications

1.1 DESCRIPTION

1.1.1 4823 Coupler

The ICS Electronics Model 4823 IEEE 488 Bus Interface Card is a general purpose card used to connect various digital devices to the IEEE 488 Bus. The 4823 Interface Card comes in a standard hardware configuration that is firmware configured for each users' application. Although the card is primarily intended for the OEM user, it is also available in a standard firmware configuration for low volume applications.

The 4823 Interface Card includes an IEEE/IEC 488 Bus Interface, eight address and control input lines, 56 parallel bi-directional I/O lines, and 11 status/data handshake lines. The 4823 firmware configures the 56 data lines into single or dual input and/or output paths. Each data path can be independently specified as having n BCD (HEX) digits or binary bytes as long as the sum of the data lines does not exceed 56. The firmware also defines the data polarity, status levels, and handshake line polarity. The 4823 Interface Card also contains four edge mounted LED indicators to aid the user in verifying proper system operation.

The 4823 Interface Card firmware is customized by entering the proper values in a table stored in the 4823 PROM. The 4823 firmware is stored in a plug-in, UV light eraseable PROM. The table contents are normally established by having the user fill out a 4823 Configuration Questionnaire to establish his requirements. The table contents are then generated by converting the questionnaire answers to binary values. Although this conversion is normally done by ICS Electronics, the user may do the conversion himself by following the guidelines in Appendix A.

The 4823 Interface Card comes with an array of accessory items to simplify the customer's installation. Two printed circuit board assemblies are available to mount the IEEE 488 Bus Connector and address switch to the host device's rear panel. Three types of 4823 mating connectors, metric studs, IEEE 488 Bus Connector, and IEEE 488 Bus Cables are part of the available accessories.

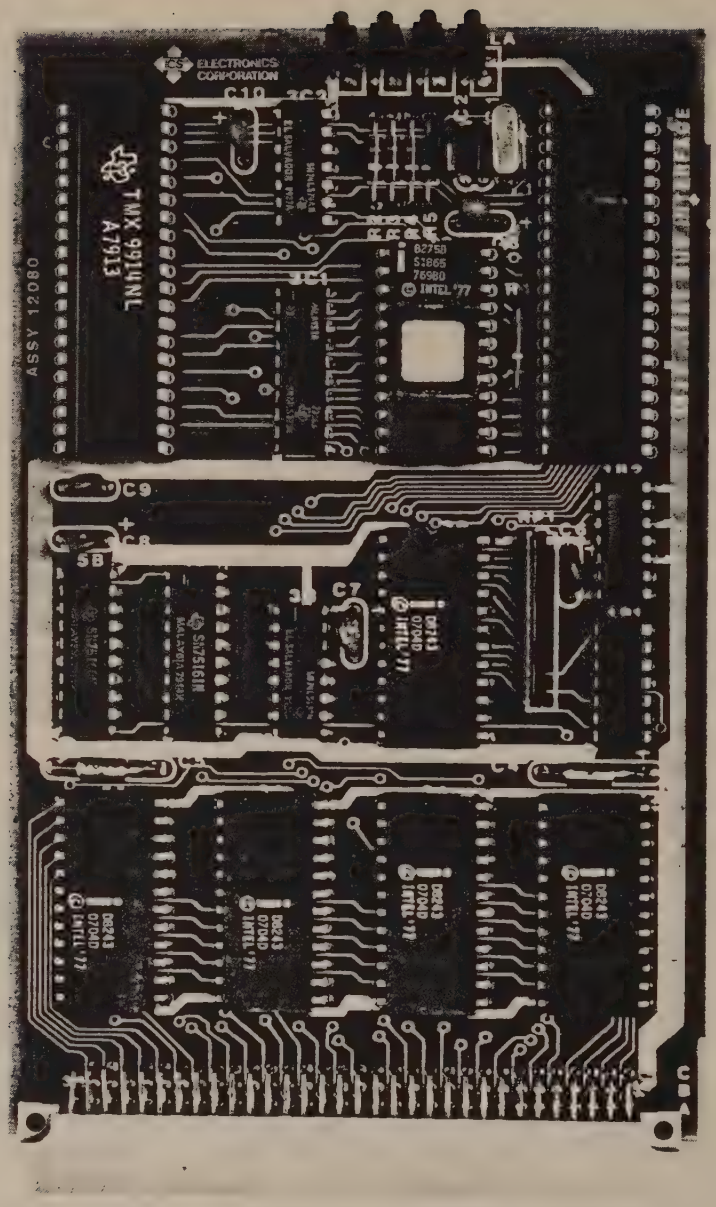


Figure 1-1 Model 4823 IEEE 488 Bus Interface Card

1.1.2 IEEE 488 BUS

The IEEE 488 Bus transfers data and commands between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel to the signal lines.

Eight of the lines (DIO1-DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, NDAC). The other five lines are for control of Bus activity.

Devices connected to the Bus may be talkers, listeners, or controllers. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO1-DIO8). Addresses are set into each device at the time of system configuration either by switches built into the device or by jumpers on a PC board. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers will be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of the five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code.* When ATN is false, any data code of 8 bits or less, understood by both talker and listener(s), may be used.

The other control lines are IFC, REN, SRQ, and EOI.

IFC (interface clear) places the interface system in a known quiescent state.

REN (remote enable) is used with other coded messages to select either local or remote control of each device.

Any device on the IEEE Bus can set the SRQ (service request) line true. This indicates to the controller that some device on the Bus wants attention, i.e., a counter that has just completed a time-interval measurement and wants to transmit the reading to the controller.

EOI (end or identify) is used by a device to indicate the end of a multiple-byte transfer sequence. When a controller sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

* American Standard Code for information interchange. Table 1-1 shows both the ASCII codes and the corresponding IEEE 488 Bus messages.

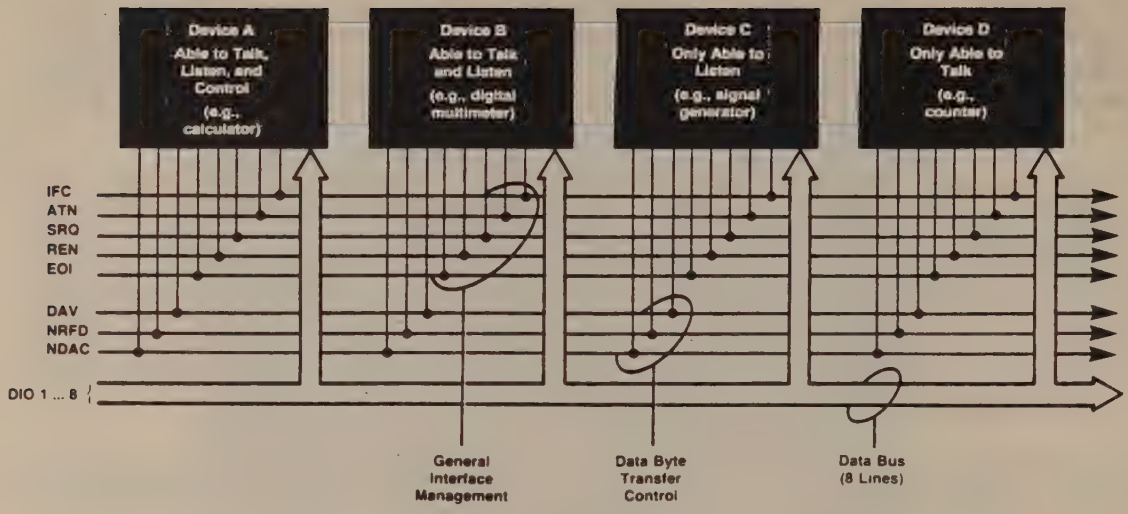


Figure 1-2 IEEE 488 BUS

TABLE 1-1 IEEE 488 COMMAND AND ADDRESS MESSAGES

ASCII — IEEE 488 BUS MESSAGES (COMMANDS AND ADDRESSES) HEX CODES

MSD / LSD	0		1		2		3		4		5		6		7	
	ASCII	MSG	ASCII	MSG	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG	ASCII	MSG
0	NUL		DLE		SP	00	0	16	@	00	P	16			p	
1	SOH	GTL	DC1	LLO	!	01	1	17	A	01	Q	17	a		q	
2	STX		DC2		"	02	2	18	B	02	R	18	b		r	
3	ETX		DC3		#	03	3	19	C	03	S	19	c		s	
4	EOT	SDC	DC4	DCL	$	04	4	20	D	04	T	20	d		t	
5	ENQ	PPC	NAK	PPU	%	05	5	21	E	05	U	21	e		u	
6	ACK		SYN		&	06	6	22	F	06	V	22	f		v	
7	BEL		ETB		'	07	7	23	G	07	W	23	g		w	
8	BS	GET	CAN	SPE	(	08	8	24	H	08	X	24	h		x	
9	HT	TCT	EM	SPD	)	09	9	25	I	09	Y	25	i		y	
A	LF		SUB		*	10	:	26	J	10	Z	26	j		z	
B	VT		ESC		+	11	;	27	K	11	[	27	k		{	
C	FF		FS		,	12	<	28	L	12	\	28	l		|	
D	CR		GS		-	13	=	29	M	13	]	29	m		}	
E	SO		RS		.	14	>	30	N	14	^	30	n		~	
F	SI		US		/	15	?	UNL	O	15	_	UNT	o		DEL	

MEANING DEFINED BY PCG CODE

MEANING DEFINED BY PCG CODE

ADDRESSED COMMAND GROUP

UNIVERSAL COMMAND GROUP

LISTEN ADDRESS GROUP

TALK ADDRESS GROUP

SECONDARY COMMAND GROUP

PRIMARY COMMAND GROUP (PCG)

Notes:

1. Device Address messages shown in decimal
2. Message codes are:
   DCL — Devices Clear
   GET — Device Trigger
   GTL — Go to Local
   LLO — Local Lockout
   PPC — Parallel Poll Configure
   PPU — Parallel Poll Unconfigure
   SDC — Selected Device Clear
   SPD — Serial Poll Disable
   SPE — Serial Poll Enable
3. ATN off, Bus data is ASCII; ATN on, Bus data is an IEEE MSG.

In the interest of cost-effectiveness it is not necessary for every device to be capable of responding to all the lines. Each can be designed to respond only to those lines that are pertinent to its function on the Bus.

1.2 DETAIL SPECIFICATIONS

The following specifications apply in general to all 4823 Interface Cards. Exact specifications for your 4823 may be found by examining the attached questionnaire for the program in your PROM. The questionnaire number is the same as the program number shown on the PROM label.

1.2.1 IEEE 488 Bus Functions

Code	Description	Comments
SH1	Source Handshake	Included
AH1	Acceptor Handshake	Included
T5, TE0	Talker	No Extended Capability
L3, LE0	Listener	No Extended Capability
SR1	Service Request	Included
PP0	Parallel Poll	Not Implemented
RL1	Remote, Local	Included
DC1	Device Clear	Included
DT1	Devices Trigger	Included
C0	Controller	Not Implemented

Interface Driver and receiver circuits are Bus compatible. Receivers contain Bus terminating resistors and have 500 mV hysteresis. Drivers are three-state devices, capable of driving up to 15 other Bus compatible devices. Power up/down protection is included to prevent transmitting invalid data to the Bus.

Format Sixteen lines, eight data and eight for control status messages. Data transfer is byte serial using a three-wire handshake per IEEE 488 Standard.

Transfer Rates Data transfer rates are typically 11K bytes/sec when talking and 5K bytes/sec when listening.

1.2.2 Parallel I/O Functions

1.2.2.1 TALKER FUNCTION

Converts user's BCD or binary input data into 8-bit characters for transmission over the Bus. Symbols or other characters can be added to the message as required. Talker function also responds to a serial poll and outputs a response word that indicates when data is present and ready to be outputted.

Input Logic Levels

Data inputs have the following voltage levels:

High = +2.0 to +5.0 Vdc @ 20 uA

Low = -0.5 to +0.5 Vdc @ 20 uA

Talker[1] Operation

Module talk channel senses the EDR input and, if addressed as a talker, inputs the data and transmits it over the Bus in the preset format. If not addressed as a talker, the module talk channel will set the SRQ line if the SRQ Enable input is high. Later, when addressed as a talker, the module talk channel will input and transmit the data over the Bus.

Input Timing

External Data Inhibit line sets within 1 usec of the active edge of the EDR Input signal and resets after data is loaded. Typical data loading time for 7 BCD/HEX characters is 2.3 msec.

1.2.2.2 LISTENER FUNCTION

Listener accepts ASCII numbers (HEX 30 - 3F, see Table 1-1) or binary characters from the Bus and converts them into parallel words with latched outputs to drive the user's equipment.

Output Logic Levels

Data stored in output latches until changed.

Latch outputs have the following output levels:

High = +2.5 to +5 Vdc @ 200 uA source

Low = 0.0 to +0.5 Vdc @ 5 mA sink

Firmware defines output word size and logic polarity.

Listener Operation

Module accepts a string of characters when addressed as a listener and transfers them to the parallel output when a terminator is sensed. Number of characters varies from 1 to the number that fills the defined ouput word size. Characters in excess of the output word size are lost.

BCD/HEX units recognize user selected characters, such as a comma, CR or a LF, as a terminating character or presence of the Bus EOI signal as a terminating condition. Binary units only recognize presence of the Bus EOI Signal or after the buffer is full, the user selected character.

---

1 Program revisions below 4.0 loaded the data into the 4823's Talk buffer when EDR is sensed (if buffer empty) and output the data when addressed to talk.

Output Timing	Typical data output time for 7 BCD/HEX characters (after receipt of terminator) is 1.5 usec. Output data stable 20 usec prior to the data transfer pulse.

1.2.3 Configurable Features

The following 4823 functions are user configurable to match the needs of the host device. The configuration is a two step process. The user first lists his requirements in the 4823 Configuration Questionnaire and then ICS uses these requirements to generate a table stored in the 4823's plug in PROM.

1.2.3.1 TALK FUNCTION PARALLEL INPUTS

Number of Channels	One or two with independent External Data Ready and Inhibit lines.
Type of Characters	Independently select BCD/HEX 4-bit nibbles or binary 8-bit characters for each channel.
Number of Characters/CH	One to 14 nibbles per channel, but not to exceed a total of 14 nibbles including the Listen Function (See Table 2-4).
Assigned Nibbles Per Channel	List of nibbles used for each channels' parallel data inputs. Do not use any nibble twice (See Table 2-4).
Data Polarity	Independently specify data polarity for each Talk channel.
Talk Character Code Conversion	Independently specify a separate BCD/HEX to ASCII code conversion table for the parallel input data (standard table shown in 1.2.4.1). Not used for binary data.
Bus Message Formats	Independently specify a separate 1 to 20 character output message for each Talk channel.
External Data Ready	Select high or low going inputs that mean the parallel data is stable and ready to be inputted into the 4823.
External Data Inhibits	Select high or low true outputs that mean the 4823 is busy inputting the parallel data. Do not change the data while these lines are in their active state.

1.2.3.2 LISTEN FUNCTION PARALLEL OUTPUTS

Number of Channels	One or two with independent data output strobe pulses.
Type of Characters	Independently select BCD/HEX four-bit nibbles or eight-bit binary bytes.
Number of Characters/CH	One to 14 nibbles per channel, but do not exceed a total of 14 nibbles including the Talk Function (See Table 2-4).
Assigned Output Nibbles	List of nibbles to be used for each Listen channel's output. Do not use any nibble twice (See Table 2-4).
Data Polarity	Independently specify data polarity for each Listen channel.
Reset State of Output Lines	Specify state of all selected Listen output lines after power turn-on or after a device clear/reset command.
Listen Data Delimiters	Independently specify one to six data delimiting characters for each channel. A delimiter is a character that the 4823 recognizes as possibly ending an input data string from the IEEE 488 Bus, i.e., 123, or 123 CR LF (see 1.2.4.2 for standard delimiters).
Listen Data Strobe	Independently specify data ready strobe polarity for each channel. Strobe pulse width is 20 usec minimum. Strobe can sink 4 standard TTL loads.

1.2.3.3 SPECIAL 488 FUNCTIONS

Device Clear, Selected Device Clear, & Reset	Upon receipt of device clear, selected device clear, when reset, or at power turn on, the module outputs the user's pre-set values to all data output lines. The module also outputs the clear strobe pulse to reset the host device. Specify Clear Strobe polarity.
Device Trigger	Upon receipt of the Bus device trigger (GET) command, the module generates a negative going trigger pulse which can be used to initiate action in the user's equipment. Trigger pulse width is 1.3 usec minimum. Trigger can sink 1 standard TTL load.

SRQ

Module generates a Bus Service Request Interrupt (SRQ) when it receives external data if not addressed as a talker. SRQs can be inhibited by grounding the SRQ Enable Switch input. The module automatically resets the SRQ signal when it is addressed to talk or when serial polled.

IFC

Unaddresses the 4823. Listen Only units require 20 usec to return to the listen only state after receiving an IFC command.

Serial Poll Response

Module responds to a serial poll by placing a unique character on the data lines to indicate whether the module needs service. The controller then can take the appropriate action to service the module. The positive response character must have the 2^6 bit on. Select one character for each Talk channel. (See 1.2.4.3 for standard response characters).

1.2.3.4 MISCELLANEOUS SIGNALS

Status 1
Status 2

Two status input lines to enable the Module to determine the condition of the user's equipment and operate the RDY indicator. Independently select status line active polarity.

ASW 1-Thru 5

Single 5-bit address switch inputs provide 31 Talk/Listen addresses (0 thru 30). Talk/Listen capabilities are mutually exclusive (unit may not talk to itself). Two additional Talk Only and Listen Only switch inputs force the module into the selected Talk or Listen Only mode. If a second channel is implemented, it is automatically given an address one count above the address switch setting. The even address is assigned to channel one and the odd address to channel two.

Logic "0" = +2.5 to +5 Vdc, LSB = ASW1.
Logic "1" = 0 to +0.5 Vdc.

TSW/LSW

Talk and Listen Only switch inputs. Same logic polarity as address switch inputs.

SISW

SRQ Enable switch input. Enable is open, Inhibit is 0 to +0.5 Vdc.

Remote

Output signal intended to disable the user's local controls. The module operates the Remote output line in response to local and remote commands received from the IEC/IEEE 488 Bus. Select signal's logic polarity. Remote output stays in local when 4823 is in the Listen Only mode.

Reset — Input resets module and causes restart of internal program. Reset is 0 Vdc at 6mA, non-reset is +2.5 to +5 Vdc.

1.2.4 Standard Configuration[2]

The 4823 Bus Interface is available in a standard configuration of one Talk and one Listen channel, 7 BCD characters per channel. The exact specifications for the standard configuration, program F31250, are listed below.

NOTE

Possible selections are shown in parenthesis and F31250[2] specifications are shown underlined.

1.2.4.1 TALK CHANNEL(S)

Number of Talk channels (1 or 2) : 1
Type of characters (BCD/HEX or binary): BCD/HEX
Number of characters (1 to 14) : 7
Assigned input lines (specify data nibbles from Table 2-4 and save low nibble numbers for Listen) :

Nibbles are: (MSD) 8,9,10,11,12,13,14 (LSD)

Data Polarity (logic 1 = high or low) : high

TALK CHARACTER CODE CONVERSION TABLE, CHANNEL #1 ONLY

BCD/HEX Input	ASCII Output	BCD/HEX Input	ASCII Output
0000	0	1000	8
0001	1	1001	9
0010	2	1010	+ (plus)
0011	3	1011	- (minus
0100	4	1100	. (period)
0101	5	1101	, (comma)
0110	6	1110	E
0111	7	1111	_ (space)

Talk output format: DDDDDDD CR LF

Where: D = Data character from conversion table
CR = Carriage Return
LF = Line Feed

External Data Ready Input (high or low going): high going
External Data Inhibit Output (high or low true) : low true

---

[2] F31250 is standard program for Revision 4.0 and later units.
F31200 is standard program for revisions below 4.0.

1.2.4.2 LISTEN CHANNEL(S)

Number of listen channels (1 or 2) : 1

Type of characters (BCD/HEX or binary) : BCD/HEX

Number of characters (1 to 14 minus talk characters) : 7

Assigned output lines (specify data nibbles from Table 2-4 and start with nibble #1) :

Nibbles are: (MSD) 1,2,3,4,5,6,7 (LSD)

Data polarity (logic 1 = high or low) : high

RESET STATE OF OUTPUT LINES TABLE

Nibble	Output (8421)	Nibble	Output (8421)
1	0000	8	N/A
2	0000	9	N/A
3	0000	10	N/A
4	0000	11	N/A
5	0000	12	N/A
6	0000	13	N/A
7	0000	14	N/A

Listen input data delimiters (ASCII characters which will terminate a Listen data message):

CR, LF, comma, N/A, N/A, and N/A.

Listen Data Strobe (logic 1 = high or low) : high

1.2.4.3 SPECIAL 488 FUNCTIONS

Clear output pulse polarity (high or low going) : low

SRQ response character code (Bit 7 must be a 1 for data ready).

CONDITION	RESPONSE CHARACTER		
	8765	4321	(HEX)
Neither channel has data available	0000	0000	00
Channel #1 Data available	0100	0001	41
Channel #2 Data available	N/A	N/A	N/A
Both channels have data available	N/A	N/A	N/A

1.2.4.4 MISCELLANEOUS SIGNALS

Status A input (logic 1 = high or low) : high
Status B input (logic 1 = high or low) : low
Reset input fixed as negative active level

Remote output active level (logic 1 = high or low) : low
Device Trigger output fixed as negative going pulse

1.2.5 Indicators

PWR	An LED which illuminates when the module has +5 Vdc power and has successfully passed power-on self test.
RDY	An LED which illuminates when the inputs on the two status lines match the user's selected logic levels.
MTA	An LED which illuminates when the module has recognized its Talk address or when it has been placed in a Talk Only mode.
MLA	An LED which illuminates when the module has recognized its Listen address or when it has been placed in a Listen Only mode.

1.2.6 Physical Description

POWER	+5 $\pm$ 0.25 Vdc @500 mA max.
SIZE	100 mmW X 160mmL X 15mmH (3.94inW X 6.30inL X 0.60inH) DIN41494 compatible
OUTLINE	Per Figure 1-3
WEIGHT	10 ounces nominal
CONNECTOR	Mates to 96-pin, (3 row x 32 pins each) DIN41612 connector
TEMPERATURE	$0^{\circ}C$ to + $70^{\circ}C$ operating in free air $-20^{\circ}C$ to + $85^{\circ}C$ storage

1.3 4823 ACCESSORY SPECIFICATIONS

1.3.1 Horizontal Connector/Switch Assembly (P/N 112084)

The 4823 Horizontal Connector/Switch Assembly is a small PCB assembly containing an IEEE 488 Bus Connector and an 8 position rocker switch assembly. The assembly is intended to be rear panel mounted inside the host device. In the horizontal configuration, the address switch is located to the right of the Bus Connector. Connections to the 4823 Interface Card are made via a 36 inch long, 26 conductor flat ribbon cable that attaches to the top of the connector/switch assembly. Over all assembly dimensions are 3.50 in. long by 1.35 in. high and 0.55 in. deep behind the panel.

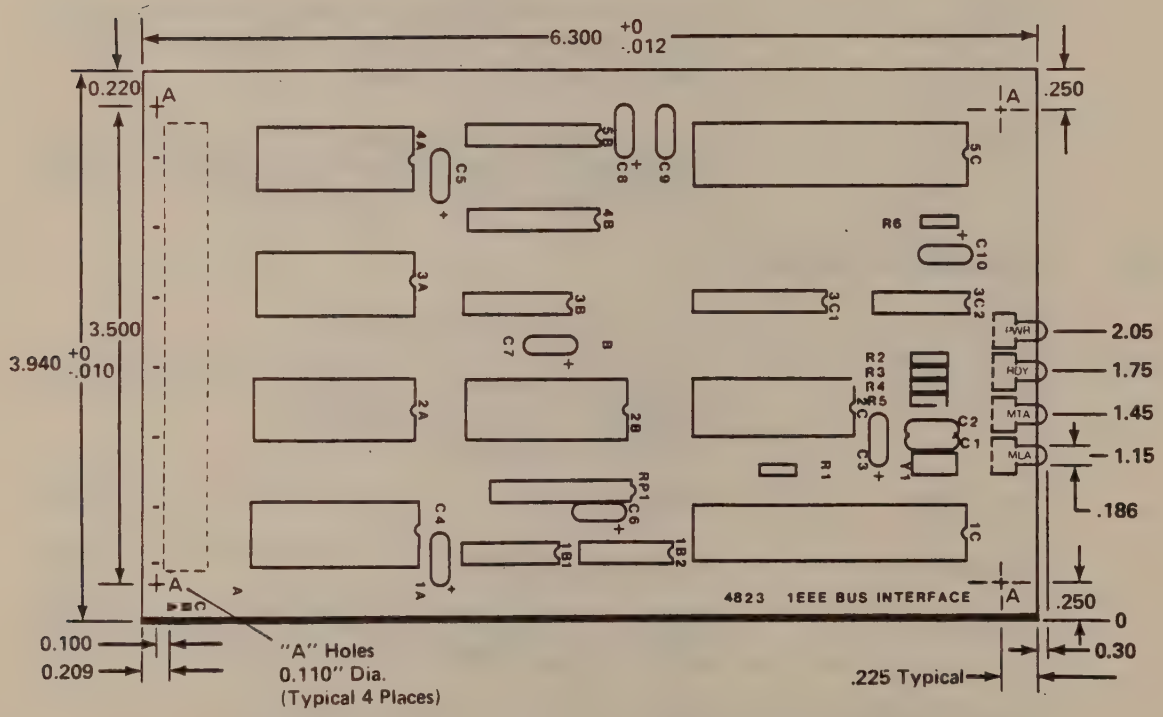


Figure 1-3 4823 Outline and Mounting Dimensions

1.3.2 Vertical Connector/Switch Assembly (P/N 112088)

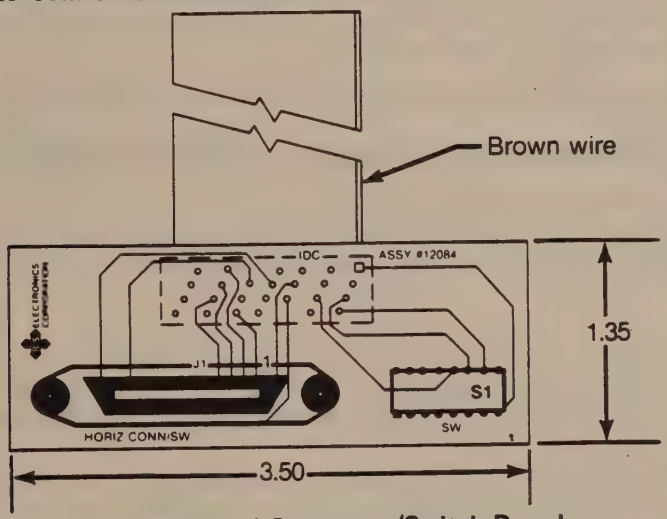
The 4823 Vertical Connector/Switch Assembly is similar to the horizontal assembly described above except that the address switch is mounted above the Bus Connector and the flat ribbon cable attaches to the left side of the assembly. Overall assembly dimensions are 3.00 in. long by 1.65 in. high and .55 in. deep behind panel.

1.3.3 Mating Connectors

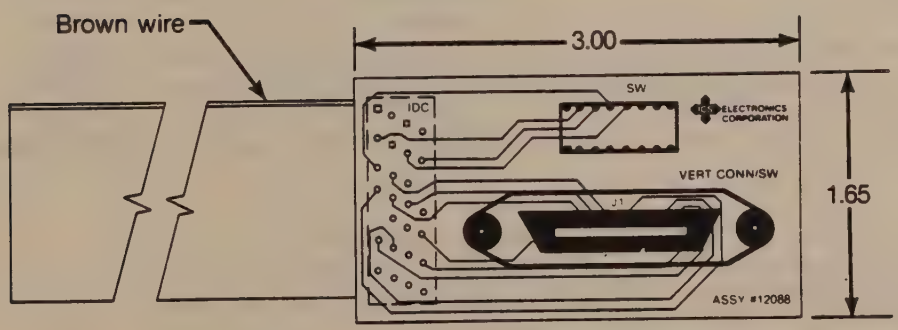
Mating connectors are available that conform to the European DIN41612 specifications. The connectors are all 96 pin, (3 rows x 32 pins/row). Termination styles include:

solder eyelet:	P/N 902023
wire wrap:	P/N 902024
dip solder:	P/N 902025

See Figure 1-4 for connector dimensions.



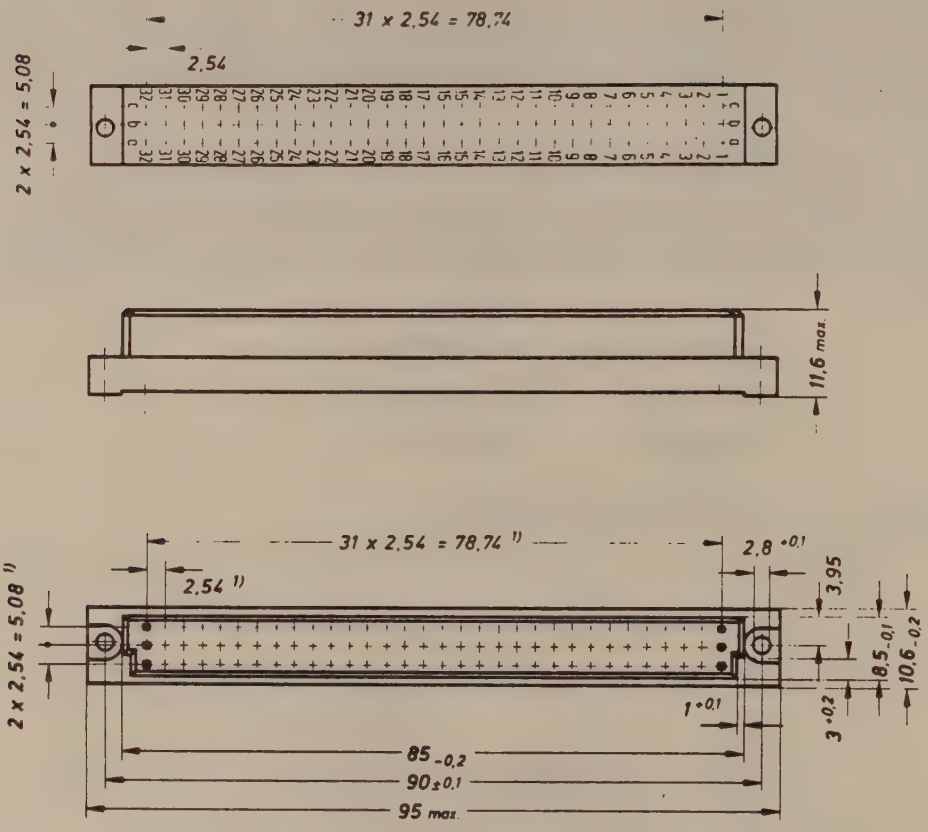
a) Horizontal Connector/Switch Board



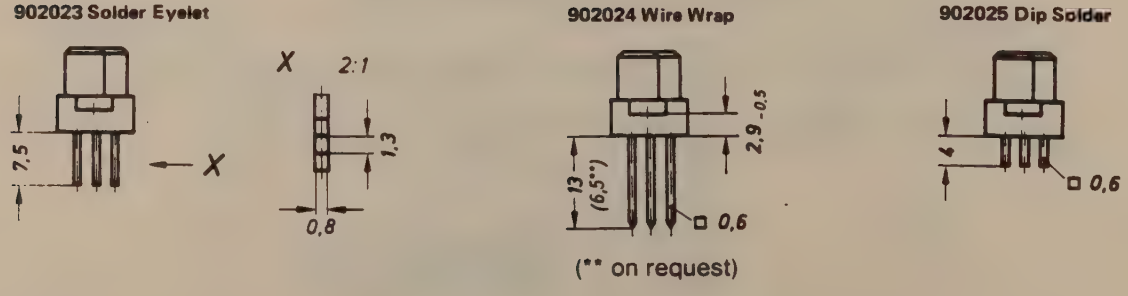
b) Vertical Connector/Switch Board

Figure 1-4 4824 Connector/Switch Boards

96 Contacts Female Connector - Three Row -



Termination Method



(** on request)

NOTE:

Dimensions in mm

1) Tolerance of center lines between any two contacts ±0.06

Figure 1-4 4823 Mating Connector Dimensions

2

Installation

2.1 UNPACKING AND INSPECTION

If shipping carton or instrument is damaged, call carrier immediately. Inspect Coupler for damage (scratches, dents, etc.). If unit is damaged or fails to meet specifications, notify ICS Electronics or area sales representative immediately. Retain shipping carton and packing material for carrier's inspection. ICS will make arrangements for unit to be repaired or replaced without waiting for claim against carrier to be settled.

2.2 CHASSIS INSTALLATION

There are several ways that the 4823 Bus Interface can be installed in an electronics chassis. The best location will depend upon the available room in a particular chassis or case. The following are the more popular mounting techniques:

1. In card guides with spacing set for a single European standard size card. Use a 3 row, 32 pins per row, DIN41612 compatible connector to mate with the 4823 Bus Interface Card.

2. Bolted to the side, rear panel, or bottom panel. Use four stand offs; two picking up the connector mounting screws and two spaced to pick up the ejector mounting holes. See Figure 1-3 for exact mounting dimensions.

3. Bolted to the outside of the rear panel and protected with a metal cover. See Figure 1-3 for board outline and mounting dimensions.

The following guidelines should be kept in mind when selecting a mounting location:

1. The card should be mounted vertically for best air flow and convection cooling. Although the 4823 Bus Interface only dissipates 2.5 watts, the cooler it runs, the longer its lifetime will be.

2. The card should be mounted so that the LED's are visible for system trouble shooting.

3. The card should not be mounted adjacent to a high gain analog circuit or one sensitive to digital clock noise without adequate shielding. The basic clock frequency in the 4823 is 3.6864 MHz.

4. The card should not be mounted on the top cover if it could be avoided or over a local hot spot as the excess heat will reduce the cards useful life.

5. Lead length from the card to the rear panel should be less than three feet (1 meter) to avoid cross talk and to avoid adding additional noise and capacitance to the IEEE Bus.

6. Power lines should be checked for excesssive noise after the card is installed and additional filtering should be added if any additional noise is discovered.

2.3 4823 CARD CONNECTIONS

The 4823 Bus Interface Card connections are broken down into four types: power, IEC/IEEE Bus Signals, address inputs, and parallel Instrument Data and Status lines. Due to the different nature of these signals, each type is covered separately in the following sections.

2.3.1 POWER CONNECTIONS

The 4823 Bus Interface requires approximately 500mA of regulated +5 Vdc + 0.2 Vdc power. The power line should be of sufficient size (24 AWG minimum) and suitably filtered to prevent voltage transients and electrical noise from the host unit from interfering with the operating of the Bus Interface. In power critical situations, the 4823's power consumption can be reduced 80 mA by removing the four LED indicators at the top of the Bus Interface Card. Table 2-1 shows the 4823's power connections.

TABLE 2-1 4823 POWER CONNECTIONS

Signal Name	4823 Pin No.	Signal Function
+5	A1	Plus 5 Volt dc input
+5	B1	Plus 5 Volt dc input
Gnd	B32	Power and logic ground
Gnd	C32	Power and logic ground

2.3.2 IEC/IEEE 488 Bus Connections

Connect the Bus output lines to a 25 pin IEC connector or to a 24 pin IEEE 488 connector as shown in Table 2-2. For the IEEE 488 Bus, use an Amphenol 57-20240 or an ICS 902004 connector. For the IEC Bus, use a Cinch DB-25P or an ICS 902007 connector. Mount the connector to the rear panel using metric studs, ICS PN 490001.

2.3.3 Address and Switch Inputs[1]

The following Bus address and mode control lines would normally be wired to a 8 position rocker switch (assuming all eight inputs are used). 4823 address inputs are ground or low true. External pull up resistors are not required since the 4823 contains its own pull up resistors. Refer to Table 2-3 for the switch input pin assignments.

TABLE 2-2 4823 IEC/IEEE BUS SIGNALS

Signal Name	4823 Pin No.	IEEE 488 Pin No.	IEC Pin No.
DIO1	B28	1	1
DIO2	C28	2	2
DIO3	B29	3	3
DIO4	C29	4	4
DIO5	B30	13	14
DIO6	C30	14	15
DIO7	B31	15	16
DIO8	C31	16	17
EOI	B23	5	6
DAV	A22	6	7
NRFD	A21	7	8
NDAC	C22	8	9
IFC	B22	9	10
SRQ	C23	10	11
ATN	B24	11	12
REN	C21	17	5
Bus Gnd	A32	18-24	18-25
Shield	A32	12	13

1 Program revisions below 4.0 were high or open true address inputs.

TABLE 2-3 ADDRESS AND SWITCH INPUTS

Signal Name	Signal Function	4823 Pin No.
ASW1	Address bit 2^0 (LSB)	C8
ASW2	Address bit 2^1	A8
ASW3	Address bit 2^2	A7
ASW4	Address bit 2^3	A9
ASW5	Address bit 2^4	C9
TSW	Talk Only Enable	B8
LSW	Listen Only Enable	B9
SISW	SRQ Enable	A6[1]
GND	Switch Common (logic 1)	C32/B32

Note: [1] If SRQ Enable is not used, jumper it to ground to inhibit interrupts on external data or leave it open to enable SRQ interrupts on presence of external data.

2.3.4 Instrument Data and Status Lines

The signals listed in Table 2-4 are used to connect the 4823 Bus Interface to the host instrument. The Data lines are all bi-directional and their functions, logic levels, and direction (input vs. output) are all established by the user's questionnaire. The status and control lines have preset functions and directions and only their logic levels are user assignable. Note that output refers to signals going out from the 4823 and input refers to those signals going into the 4823 Bus Interface.

2.3.5 Power-On-Reset

It is strongly recommmended that the Reset (RST) input be held in the reset state (0 Vdc) until after the 5 volt line is completely stable. There is a power on reset circuit on the card, but by holding the Reset low at power turn on, there can be no chance of a bad power-on reset with a slow rising power supplier.

TABLE 2-4

INSTRUMENT DATA AND STATUS LINES

Signal Name	4823 Pin No.	Signal Function	
CH1	A30	1	
CH2	A29	2	Data Nibble #1
CH3	A28	4	
CH4	A27	8	
CH5	A31	1	
CH6	A26	2	Data Nibble #2
CH7	C27	4	
CH8	B27	8	
CH9	A25	1	
CH10	C26	2	Data Nibble #3
CH11	B26	4	
CH12	C25	8	
CH13	C24	1	
CH14	A23	2	Data Nibble #4
CH15	A24	4	
CH16	B25	8	
CH17	A19	1	
CH18	A20	2	Data Nibble #5
CH19	C20	4	
CH20	B21	8	
CH21	B20	1	
CH22	B15	2	Data Nibble #6
CH23	C15	4	
CH24	B16	8	
CH25	C16	1	
CH26	A17	2	Data Nibble #7
CH27	C18	4	
CH28	A18	8	
CH29	A16	1	
CH30	B17	2	Data Nibble #8
CH31	C17	4	
CH32	B18	8	
CH33	B14	1	
CH34	C14	2	Data Nibble #9
CH35	A15	4	
CH36	A14	8	

TABLE 2-4

INSTRUMENT DATA AND STATUS LINES
(Continued)

Signal Name	4823 Pin No.	Signal Function
CH37	A13	1
CH38	C13	2
CH39	B13	4 — Data Nibble #10
CH40	C12	8
CH41	B12	1
CH42	A12	2
CH43	C11	4 — Data Nibble #11
CH44	B11	8
CH45	A10	1
CH46	B10	2
CH47	C10	4 — Data Nibble #12
CH48	A11	8
CH49	B6	1
CH50	C6	2
CH51	B7	4 — Data Nibble #13
CH52	C7	8
CH53	C5	1
CH54	B5	2
CH55	C4	4 — Data Nibble #14
CH56	B4	8
EDR1	A5	Talk Ch #1, Ext. Data Ready input
EDR2	A3	Talk Ch #2, Ext. Data Ready input
INH1	A4	Talk Ch #1, Data Inhibit output
INH2	A2	Talk Ch #2, Data Inhibit output
STATA	C3	Unit Ready Status A input
STATB	B3	Unit Ready Status B input
REM	C1	Unit Remote Mode Control output
CLR	B2	Unit Clear/Reset Pulse output
DATA 1	C2	Listen Ch #1, Data Transfer Strobe output
DATA 2	(1)	Listen Ch #2, Data Transfer Strobe output
TRIG	C19	Device Trigger, Negative going pulse output
RST	B19	4823 Reset, Negative going pulse input

Notes: (1) Listen Channel #2's Data Transfer Strobe replaces the address switch input LSB on pin C8 when two listen channels are used.

2.4 CONNECTOR/SWITCH BOARD INSTALLATION

Both the Horizontal and Vertical Connector/Switch Board Assemblies are designed to be mounted on the inside surface of the host device's rear panel. They are fastened to the rear panel by the two metric studs. The following are the suggested installation steps:

1. Select the appropriate panel cutouts from Figure 2-2.

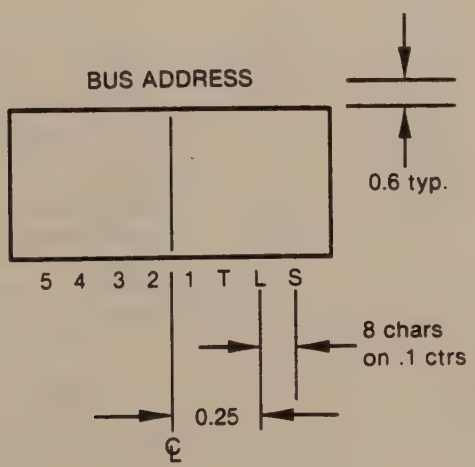
2. Locate the necessary blank area on the host device's rear panel leaving enough room for the flat ribbon cable bend radius.

3. Machine the rear panel cutouts.

4. Install the Connector/Switch Assembly from the inside, pressing the metric studs and 2 thin lockwashers to hold the connector/switch assembly to the panel.

5. Lay the flat ribbon cable in the host device chassis. Cut off excess cable and wire to the connector as shown in Table 2-5. The schematic diagram for the Connector/Switch Board is shown in Figure 7-2.

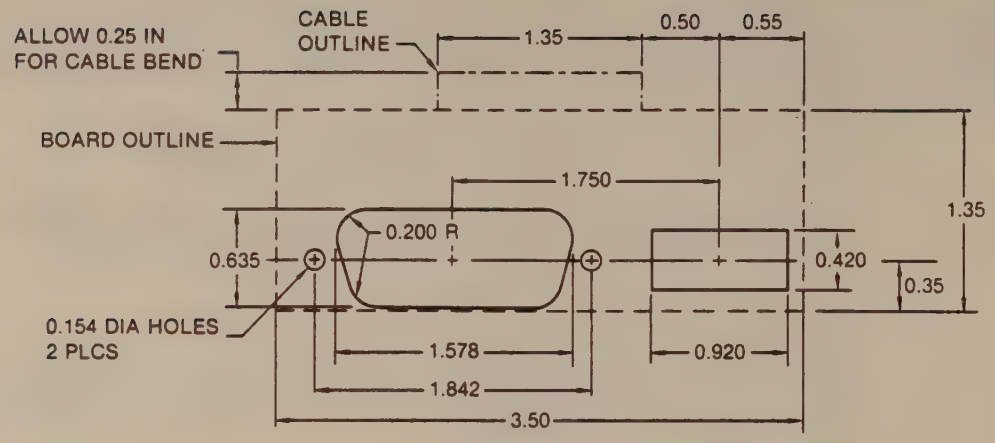
6. Mark or silk screen the switch functions on the rear panel as shown in Figure 2-1. The switch is positioned so the On (up) position connects the appropriate 4823 input signal to ground and is the logic '1' position.



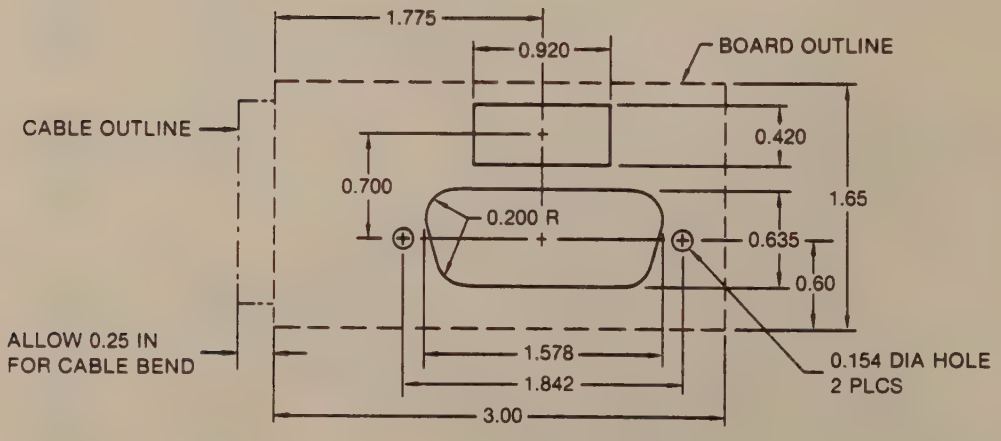
SILKSCREEN DETAIL

Center titles over openings
All letters are helvetica medium

Figure 2-1 Switch Silkscreen Detail



Horizontal Connector/Switch Board Cutouts



Vertical Connector/Switch Board Cutouts

Figure 2-2 Connector/Switch Board Panel Cutouts

TABLE 2-5 4823 TO CONNECTOR/SWITCH BOARD CONNECTIONS

Memonic	4823 Pin No.	Board Cable Color
GND	C32	BRN 1
SISW	A6	BLU 1
ASW3	A7	GRAY 1
ASW2	A8	WHT 1
LSW	B8	YEL 1
ASW1	C8	VIO 1
ASW4	A9	GRN 1
TSW	B9	ORG 1
ASW5	C9	RED 1
NRFD	A21	BLK 1
REN	C21	BRN 2
DAV	A22	RED 2
IFC	B22	ORG 2
NDAC	C22	YEL 2
EOI	B23	GRN 2
ATN	B24	BLU 2
SRQ	C23	VIO 2
DIO1	B28	GRAY 2
DIO2	C28	WHT 2
DIO3	B29	BLK 2
DIO4	C29	BRN 3
DIO5	B30	RED 3
DIO6	C30	ORG 3
DIO7	B31	YEL 3
DIO8	C31	GRN 3
BUS GND	A32	BLU 3

3

Operation

3.1 INDICATORS

The 4823 Bus Interface Card has four LED indicators mounted on the edge of the PCB opposite the connector. These four indicators are intended to act as trouble shooting aids in the event of a system malfunction. The four indicators are:

PWR	Power Indicator, on when +5 Vdc has been applied to the card, the microprocessor is running and the 4823 has successfully completed its power-on self test.
RDY	Ready Indicator, on when the Status A and Status B are held at their assigned levels.
MTA	My Talking Address Indicator, on whenever the card has recognized its Talk address on the IEEE 488 Bus or is in the Talk Only state. Goes off when the 4823 recognizes another Talk address, its Listen address, or the Untalk command.
MLA	My Listening Address Indicator, on whenever the card has recognized its Listen address on the IEEE 488 Bus or is in the Listen Only state. Goes off when the 4823 recognizes its Talk address or the Unlisten command.

3.2 SWITCH INPUTS

3.2.1 Address Switch Inputs

The address switch inputs set the card's address and establishes the automatic address, Talk Only or Listen Only address modes. These inputs are read and saved after a reset condition and are used during coupler operation. Changing these inputs during operation will have no affect unless the Reset input is momentarily grounded or the power momentarily turned off.

For AUTO ADDRESSING, pick an unused Bus address between 0 and 30 decimal. Convert the address to binary. Starting with the least significant address bit, ASW1, switch the card input to ground if it is a Logic '1' or open it if it is a Logic '0'. Leave the Talk and Listen Only inputs open. In the auto addressing mode, the card will respond to the Talk and Listen addresses sent over the Bus to it by the system controller.

For units with dual address Talk or Listen channels, use only the even addresses and disregard the least significant address bit (ASW1) as this is now the Data 2 Output. The first channel is represented by the selected even address. The second channel is automatically the next higher channel number.

CAUTION - DO NOT SET DUAL CHANNEL UNITS TO ADDRESS 30.

For TALK ONLY, set the Talk Only Enable input to ground and the Listen Only Enable input open. In the Talk Only mode, any data received by the card will be immediately formatted and passed onto the Bus.

For LISTEN ONLY, set the Listen Only Enable input to ground and the Talk Only Enable input open. In the Listen Only mode, any data received from the Bus will be immediately formatted and placed in the parallel output latches.

CAUTION

DO NOT use Talk Only or Listen Only modes with cards programmed for two talk or two listen channels.

3.2.2 SRQ Switch Inputs

For SERVICE REQUEST INTERRUPTS (SRQ's), set the SRQ Enable input open. The 4823 Bus Interface will automatically send the SRQ message over the Bus whenever external data is present and the 4823 is not addressed as a talker. To inhibit the SRQ message, ground the SRQ Enable input.

3.3 OPERATING INSTRUCTIONS

3.3.1 Pre-Operation Set-Up

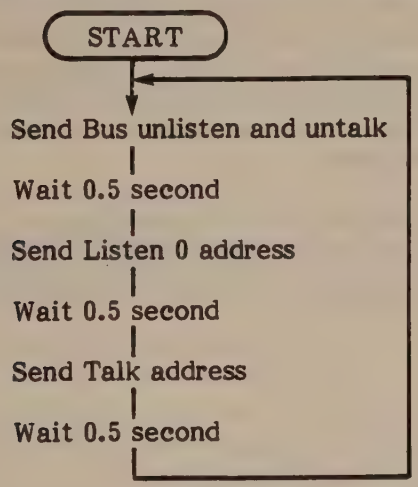
Before using the 4823 Bus Interface, design and fabricate the wiring harness assembly that connects the 4823 to the IEEE 488 Bus, the address switch, to the host device electronics and to +5 Vdc power. Install the Interface card and attach the host device to the IEEE Bus and Bus controller.

3.3.2 Initial Checkout

Turn the host device on to apply power to the 4823. The 4823's PWR indicator should come on. If the PWR indicator is not on, stop and check the 4823 for +5 Vdc power and the other items listed in the fault isolation table in Section 5.

Secondly, check the operation of the 4823's RDY indicator by switching the host device's status lines where possible. Verify that the light is on when the status inputs match the levels defined in the questionnaire.

Next, verify the address switch connections by setting the address to zero and implementing the following program on your Bus controller. The MLA and MTA indicators should sequence on and off in 0.5 second intervals.



Repeat the above test for addresses 1, 2, 4, 8, and 16 to independently test the five address switches.

Verify that the host device receives the proper response from the following Bus commands as they apply to your device.

a) Device Trigger

b) IFC, Device Clear, and Selected Device Clear

c) Remote/Local Control

Next, verify the 4823's parallel output to the host device. Check initial outputs vs. those specified in the questionnaire. Program the Bus controller to send the 4823 the proper data strings to exercise all of its parallel outputs. If your 4823 is programmed for 2 Listen channels, set the address switches to an even address value. Have the Bus controller use the even address for channel #1 and the next higher odd address for channel #2.

Finally, verify the 4823's parallel input capability. Have the host device pulse the 4823's External Data Ready line. The Bus SRQ line should become active on the selected edge of the External Data Ready pulse (if SRQ is enabled). Have the Bus controller read the data from the 4823. Verify that the format matches the questionnaire. Perform a serial poll when the SRQ line is on and off, verifying that the controller receives the proper status character. Again, for 4823's with two talk channels, set the address switch to an even value and use the even number to address channel #1 and the next higher odd number to address channel #2.

3.3.3 Manual Preparation Instructions

Adequate instructions should be included in the host device's manual to enable the end user to operate the host device thru the 4823 Bus Interface. All Bus commands should be described in terms of their effect upon the whole device, not just the 4823 Bus Interface. Bus input and output data formats should be thoroughly explained to avoid user confusion. The manual should also contain the different Bus message sequences necessary to operate or obtain data from the host device. It is also advisable to include copies of sample operating programs in the manual if they are available.

To aid the OEM user in preparing his manual, any or all portions of this manual may be reproduced in the host device's manual as described in the Copyright Waiver on the rear of the inside front page of this manual.

4

Theory of Operation

4.1 BLOCK DIAGRAM DESCRIPTION

The 4823 Bus Interface Block diagram is shown in Figure 4-1. The 4823 Bus Interface contains three major elements, all connected to a single chip microprocessor. The first element is a 2K X 8 PROM which contains the 4823's operating program and program configuration table. The second element is the IEEE 488 Bus Interface which handshakes with the Bus and enables the microprocessor to communicate with the IEEE 488 Bus. The third element is a series of Expander Buffer/Latches which store parallel output data for operating the host device and the LED Indicators. The Expander Buffer/Latches are also used to input data, switch, and status information from the host device. The EDR Logic block converts short External Data Ready pulses into levels and also generates the Inhibit signals which the host device uses to block any data change until all the data has been loaded into the 4823.

4.2 DETAILED LOGIC DESCRIPTION

4.2.1 Microprocessor Functions and Timing

The 4823 Bus Interface uses an 8039 Microprocessor to route data and make all of the operating decisions in accordance with the instructions stored in a table in a plug-in UV eraseable PROM. The 8039 Microprocessor is one member of the 8048 series of microprocessors made by Intel Corporation and National Semiconductor. Although the 8039 has an expanded internal RAM memory of 128 bytes and uses external program memory, the rest of its specifications are identical to the high speed 8048 microprocessors made by either company. The user is therefore referred to either company's 8048 User's Manual for a thorough description of the microprocessor's operation, its I/O characteristics, and data, transfer timing diagrams.

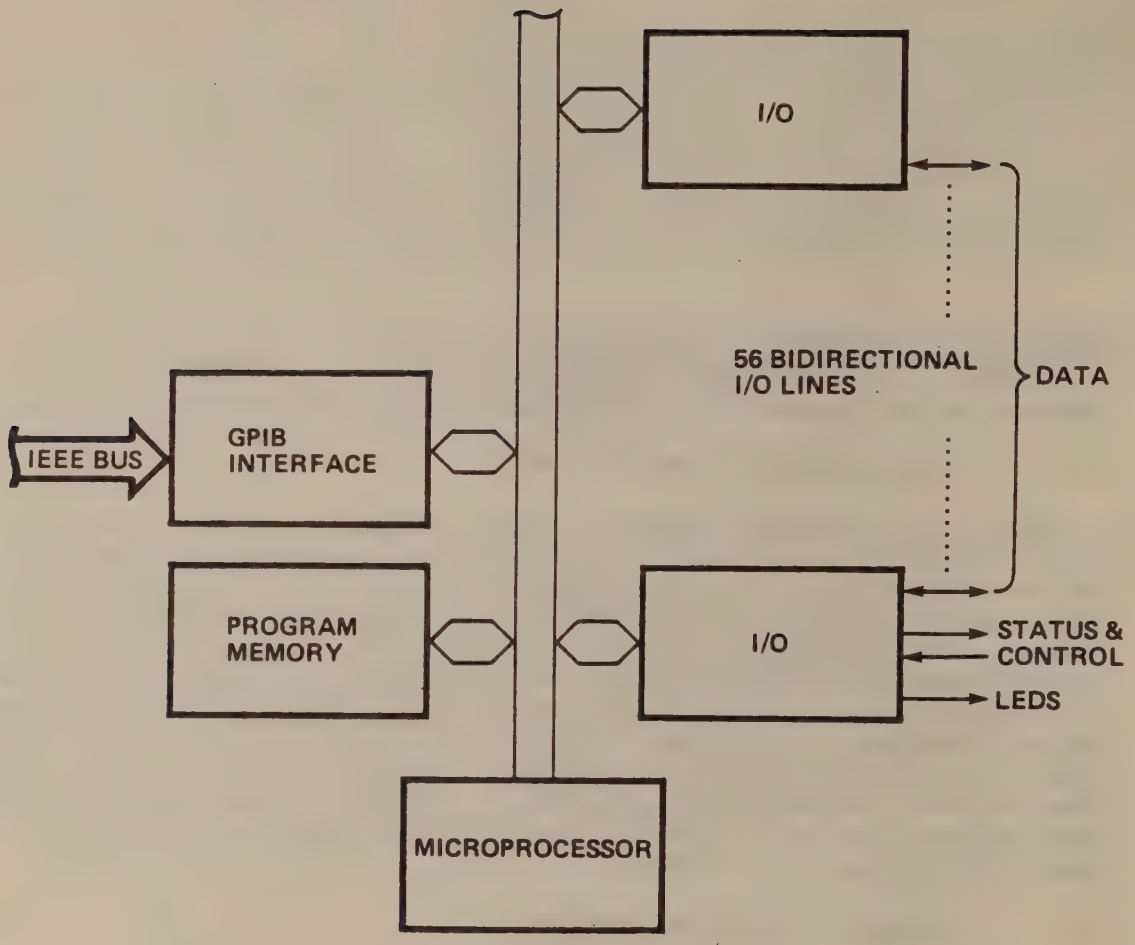


Figure 4-1 4823 Block Diagram

4.2.2 4823 Logic Diagram Description

Refer to Figure 7-1, sheets 1 and 2.

Crystal, Y1, causes the microprocessor, 1C, to internally generate an 11.0592 MHz clock pulse. This clock pulse is divided by three and becomes the T0 clock output on 1C pin 1. The T0 clock output is routed to the GPIB chip, 5C, where it is used as the clock input on 5C-18.

PROM, 2C, contains all program information for the 4823 Bus Interface. During a microprocessor fetch cycle, the lower eight bits of address information are stored in octal latch, 3C1, during the microprocesssor's ALE time. The higher order 3 address bits are latched in port 2, output bits 0, 1, and 2. Data is then inputted from the PROM during PSEN time.

The GPIB chip, 5C, performs all of the IEEE 488 Bus handshaking functions and passes data to and from the microprocessor under interrupt control. Initialization data is loaded into 5C from the data Bus. The GPIB chip's internal registers are addressed by the three least significant address bits held in latch, 3C1. The microprocessor's write control pulse, $\overline{WR}$, in conjunction with PSEN and $\overline{ALE}$ enables the GPIB chip to accept data. Data is outputted from the GPIB chip by raising DBIN (microprocessor read control $\overline{RD}$ going low) during the same PSEN and $\overline{ALE}$ time. The GPIB interrupts the microprocessor by lowering its interrupt output, INT, when it needs service. IEEE Bus data and signals are transmitted and received via Bus Tranceivers, 4B and 5B, which have internal IEEE 488 Bus terminating networks. Gate, 3C2, converts the positive going GPIB TRG signal to a negative pulse to trigger the host device.

Parallel data is transferred to and from the microprocessor as four bit nibbles on the lower four bits of the Port 2 Bus. The data is gated from the Port 2 Bus thru five I/O Expanders, 1A-4A and 2B, and latched in the same I/O Expanders to drive the host device, LED Indicators or EDR logic elements. The desired I/O Expander is addressed by a four bit character latched in the 4 least significant bits of Port 1. Decoder, 3B, converts the 4 bits to a single negative going select line which enables the desired I/O Expander. During the negative edge of the PROG signal, the Port 2 lines contain the I/O Expander's internal port address and function. Data is passed between the microprocessor and the I/O Expander on the positive edge of the PROG signal.

Exclusive 'OR' gates, 1B1, invert or pass the external data ready signals, EDR1 and EDR2, onto D-latches, 1B2. The latch outputs are inverted by a second set of exclusive 'OR' gates to generate the Data Inhibit signals. Signals CP1-CP4 from I/O Expander 2B reset the D-latches and select the EDR and Inhibit signal polarity.

5

Maintenance

5.1 INTRODUCTION

This section describes the maintenance and troubleshooting procedures for the Model 4823 Bus Interface. The 4823 does not require periodic calibration and has no internal adjustments. This section also includes a brief description of the 4823's logic conventions and symbols.

5.2 TROUBLESHOOTING PROCEDURES

This section describes procedures for locating and correcting basic Bus Interface problems. It is assumed that the user has a good grasp of his overall system, especially the interface requirements for the host device, and has familiarized himself with the basic operation of the IEEE 488 Bus and the 4823 Bus Interface.

Use the Fault Isolation steps in Table 5-1 to narrow down the problem to a specific area. The majority of initial installation problems can be fixed by following the table and making the necessary corrections to the 4823 - host device hookup, Bus controller program or to the 4823 configuration table. Field failures can be isolated by first substituting a known good 4823 to isolate the problem down to the suspect 4823. Secondly, either use the table to further isolate the problem down to the IC level or return the card to ICS for repair. Follow the warranty instructions on the back of the first page when returning a unit to ICS.

5.3 LOGIC CONVENTIONS

The unit uses positive logic, which means the normally active or high signal state is +3.5 $\pm$ 1 volts and the inactive or low state is 0 $\pm$0.5 volt. The high state is referred to as logic 1 and the low state is logic 0. The terms true and false relate to the signal being in or out of its active state and normally correspond to logic 1 and 0. However, for some signals such as the input of a OR gate, the true or active state is the low signal level (0 volts).

Complements of signals are indicated by an F or N suffix or by an inversion dot on the logic symbol. Complements of signals are indicated by an F or N suffix or by an inversion dot on the logic symbol. Complemented signals are always low when the original signal is high and vice versa. See Figure 5-1 for the standard logic symbols.

TABLE 5-1 MODEL 4823 FAULT ISOLATION STEPS

Symptom	Possible Fault	Check
No lights or PWR light off	+5 Vdc power	Power connection, external power switch
	Broken LED	Check PWR LED
	Broken Crystal	Check Y1 for rattle noise and/or sine-wave outputs
	Self test failure indicating a 4823 internal fault	
	MLA Only on	Address switch set to 30 or 31
	MTA and MLA on	Talk Only and Listen Only switches
	RDY Only on	PROM failure
	Other conditions	4823 card by substitution
RDY LED off	Host device status line levels	Status lines vs. 4823 configuration questionnaire
	Broken LED	RDY LED
No MTA or MLA LED response	Wrong Address	Address switch setting
		Value in Controller program
	Extended address on the Bus	Controller program
	T Only or L Only input low	Switch setting or device connections

TABLE 5-1 MODEL 4823 FAULT ISOLATION STEPS - Continued

Symptom	Possible Fault	Check
MTA LED on	T Only input low	Switch or device wiring
	No data sent to controller	Device input or EDR pulse missing
	Controller missing terminating character	4823 questionnarie or controller program
	Untalk or Listen address not sent	Controller program
MLA LED on	L Only input low	Switch or device wiring
	Unlisten or Talk Address not sent	Controller program
Unwanted SRQ's	SRQ ENA input high	Switch or device wiring
	Noise on EDR input lines	EDR latches and EDR input lines for noise spikes or cross-talk
Missing trigger pulses	Device trigger not sent correctly	Controller program
	Wiring error	Host device wiring harness
Missing 4823 parallel output data	Wiring error	Verify 4823 pin numbers vs questionnaire
	IC failure	Appropriate I/O Expander IC

TABLE 5-1 MODEL 4823 FAULT ISOLATION STEPS - Continued

Symptom	Possible Fault	Check
Missing 4823 data transfer strobe	Wiring error	Host device wiring
	Missing Terminator	Controller program or 4823 questionnaire
Missing 4823 input data on the Bus	EDR signal not received	Check EDR signal polarity and presence of active edge
		Host device or wiring
	Expected signal polarity	4823 questionnaire
	EDR IC failure	EDR logic elements, I/O Expander
Garbled data on the Bus	IC failure	Appropriate I/O Expander IC
	Input error	Host device or wiring
	Unexpected format conversion or data polarity	4823 questionnaire
	Unexpected or missing terminator	Controller program

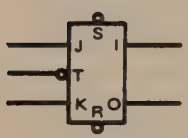
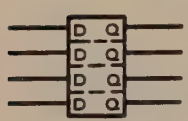
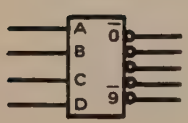
o	Inversion dot	Part of a larger symbol. Indicates that the input or output signal is low when in the active or true state.
	Open collector bar	Bar on output indicates an open collector device without an internal signal pullup.
	NAND gate	Performs the NOT-AND function. Output is low when all inputs are high.
	NOR gate	Performs the NOT-OR function. Output is high when one or more inputs are low.
	Wired OR	Performs an OR function using only chassis wires. Output low when one or more inputs are low.
	Amplifier, (level shifter or inverter)	Performs signal current amplification or level shift function. Signal polarities shown by inversion dots.
	Inverter	Performs a logic signal inversion; always used with the inversion dot.
	Clocked Flip-Flop	Output changes state on negative edge of clock if J and/or K was true during clock time. Outputs set or reset if either Preset or Reset input grounded.
	Quad Latch	Four D or storage flip-flops in single package. Normally has both Q and $\bar{Q}$ outputs. Data loads while clock high, latched when low.
	Counter	Four cascaded flip-flops in a single package designed as a counter. Divides by 10, 12, or 16. Check an IC catalog for reset, clear and load signal definitiions.
	Decoder	Four line BCD to ten line decimal decoder. Outputs low when active.

Figure 5-1 Standard Logic Symbols

6

Parts List and Location

6.1 INTRODUCTION

This section contains all information necessary to locate, identify, and order parts. The listing of parts and information for an exact replacement are shown in the attached parts list. All components locations are identified by reference designators in the parts list and in the attached circuit board assembly drawing, Figure 6-1.

6.2 REPLACEMENT PARTS

6.2.1 Standard Parts

All parts can be purchased directly from ICS Electronics Corporation, at current market price, plus a handling charge. However, since most parts are standard electronic components, it is suggested that they be secured locally for prompt replacement. The parts list gives all pertinent information including the recommended manufacturers. Where not noted, equivalent parts meeting the original part specifications may be substitued. A list of manufacturers by abbreviations is given in Table 6-1 and recommended spare parts in Table 6-2.

6.2.2 Special Parts

Parts marked with a Data Works, Fairchild Instrumentation, or an ICS part number should be procured directly from ICS Electronics Corporation. These parts are manufactured or selected to satisfy specific requirements. Substitution of other parts might not yield equivalent performance and will void any warranty.

6.2.3 Parts Ordering Information

All orders should be directed to ICS Electronics Corporation, at the address shown on the front page, or to ICS Electronics in care of your local representative. When ordering, be sure to include the following information:

a. Part description and reference designator
b. Part number, manufacturer, and stock number
c. Instrument model, serial number, and program revision level.

TABLE 6-1 List of Manufacturers by Abbreviations

Abbreviations	Company
ABC	Allen Bradley, Milwaukee, WI
ACT	Advanced Components Technology, Inc., Redwood City, CA
AEP	Alco Electronic Products, Inc., Lawrence, MA
AMA	Amaton, New Haven, CT
AMD	Advanced MicroDevices, Sunnyvale, CA
AMP	Amp Incorporated, Harrisburg, PA
ANS	Ansley Electronics Corp., Los Angeles, CA
APH	Amphenol Corp., Oakbrook, IL
ARC	Arco, Commack, NY
ARI	Aries Industries, Inc., Gardena, CA
AUG	Augat Inc., Attleboro, MA
BEC	Beckman, Heliport Division, Fullerton, CA
BEL	Belden Corp., Richmond, VA
BOR	Bourns, Riverside, CA
BUD	Budwig, Los Angeles, CA
BUS	Bussmann, Earth City, MO
CAC	Circuit Assembly Corporation, Costa Mesa, CA
CAN	Cannon, Santa Ana, CA
CEL	Cellotape, Sunnyvale, CA
CHY	Cherry Electrical Products Corp., Highland Park, IL
CJO	Cinch Manufacturing Co., Elk Grove Village, IL
CMS	Component Manufacturing Service, Bridgewater, MA
CDE	Cornell Dublier, Newark, NJ
CNT	Centralab, Los Angeles, CA
COR	Corcom Inc., Chicago, IL
CRN	Corning Glass Works, Corning, NY
CTS	CTS Corporation, Elkhart, IN
DAL	Dale Electronics Incorporation, Columbus, NB
DIA	Dialco, Brooklyn, NY
DWI	Data Works Instrumentation, (See ICS)
EPI	Epitek, Kanata, Ontario, Canada
ERI	Erie Technological Products, Erie, PA
EXL	Excel, Chicago, IL
FCL	Freedom Crystal Lab, Freedom, CA
FIS	Fairchild Inst. & Controls Div., (See ICS)
FLK	Fluke, Santa Clara, CA
FSC	Fairchild Semiconductor Div., Mountain View, CA
GHI	Grayhill, La Grange, IL
GOR	Gordos Corporation, Bloomfield, NJ

TABLE 6-1 List of Manufacturers by Abbreviations - Continued

Abbreviations	Company
HEY	Heyboer, Grand Haven, MI
HHS	Herman H. Smith, Inc., Brooklyn, NY
HP	Hewlett-Packard, Palo Alto, CA
ICS	ICS Electronics Corporation, San Jose, CA
IER	International Electronics Research Corporation, Burbank, CA
INL	Intel, Sunnyvale, CA
IRC	TRW/IRC Resistors, Philadelphia, PA
ITT	ITT General Controls, Glendale, CA
JAR	Jarome Wire, Mountain View, CA
KEM	Kemet, Greenville, SC
KOS	Koszeigi, South Bend, IN
LFS	Little Fuse Inc., Des Plaines, IL
LOP	Zollin J. Lopaugh, San Francisco, CA
LYN	Lyntron, Inc., Burbank, CA
MED	Meadows Manufacturing, Sunnyvale, CA
MIN	Minicomputer Accessories, Sunnyvale, CA
MLX	Molex Products Co., Downers Grove, IL
MON	Monsanto, Palo Alto, CA
MOT	Motorola Semiconductor Products, Inc., Phoenix, AZ
MPI	Micro Plastics Inc., Chatsworth, CA
MSC	Master Specialities Co., Costa Mesa, CA
NAT	National Semiconductor Ltd., Plattsburgh, NY
NIC	Nichicon, Chicago, IL
PAN	Panduit, Tinley Park, IL
PCL	Precision Crystal Lab, Santa Monica, CA
PNS	Panasonic, Secaucus, NJ
RAY	Raytheon, Mountain View, CA
RCH	Richlock, Chicago, IL
RGA	RG Allen, Van Nuys, CA
SAE	Stanford Applied Engineering, Long Beach, CA
SCN	Scanbe, El Monte, CA
SEK	Seiko Circuits, Sunnyvale, CA

TABLE 6-1 List of Manufacturers by Abbreviations (Continued)

Abbreviations	Company
SHO	Shoin, Japan
SIG	Signetics Corp., Sunnyvale, CA
SMN	Siemens, Iselin, NJ
SPC	Spectra Strip
SPR	Sprague Electronics, Chicago, IL
SWC	Switchcraft, Inc., Chicago, IL
TEK	Tektronics, Inc., Beaverton, OR
TEM	Temple Industries, Inc., Tecate, CA
TEX	Textool, Irving, TX
THC	Thermalloy Co., Dallas, TX
TI	Texas Instruments, Semiconductor Div., Dallas, TX
UCC	United Chem-Com, Rosemont, IL
USE	USECO, Van Nuys, CA
VIK	Viking, Chatsworth, CA
WDC	Western Digital Corp., Newport Beach, CA
WFD	Wakefield Engineering, Inc., Wakefield, MA
WIN	Winchester, Oakville, CT
ZIL	Zilog, Inc., Cupertino, CA

6.3 PARTS LISTS

The Recommended Spare Parts List (Table 6-2) contains the recommended spare parts for ten units.

The 4823 Parts List (Table 6-3) contains all components that make up the unit.

The parts list table contains both the ICS Electronics Corporation stock numbers and the manufacturers' true part numbers where applicable. True manufacturers' part numbers are not shown for industry standard parts nor items unique to the 4823 Bus Interface.

TABLE 6-2 4823 RECOMMENDED SPARE PARTS LIST

Stock Number	Qty. Per 10 Units	Description	Mfgr.	Mfgr.P/N
798039	1	IC, CPU 8039	INL	8039 - 6
792716	1	IC, PROM	ICS	-
742373	1	IC LATCH, 8 bit	TI	74LS373
742000	1	IC QUAD NAND	TI	74LS00
799914	1	IC, GPIB	TI	TMS9914NL
742086	1	IC, EX OR	TI	74LS86
742074	1	IC, DUAL D F/F	TI	74LS74
798243	2	IC, I/O EXPANDER	INL	8243
742138	1	IC, DCDR	TI	74LS138
735161	2	IC BUS XCVR	TI	75161
735160	2	IC BUS XCVR	TI	75160
701003	2	LED, RED RT ANGLE	DIA	550-0405
904003	1	CRYSTAL 11.0596 MHz	ICS	-

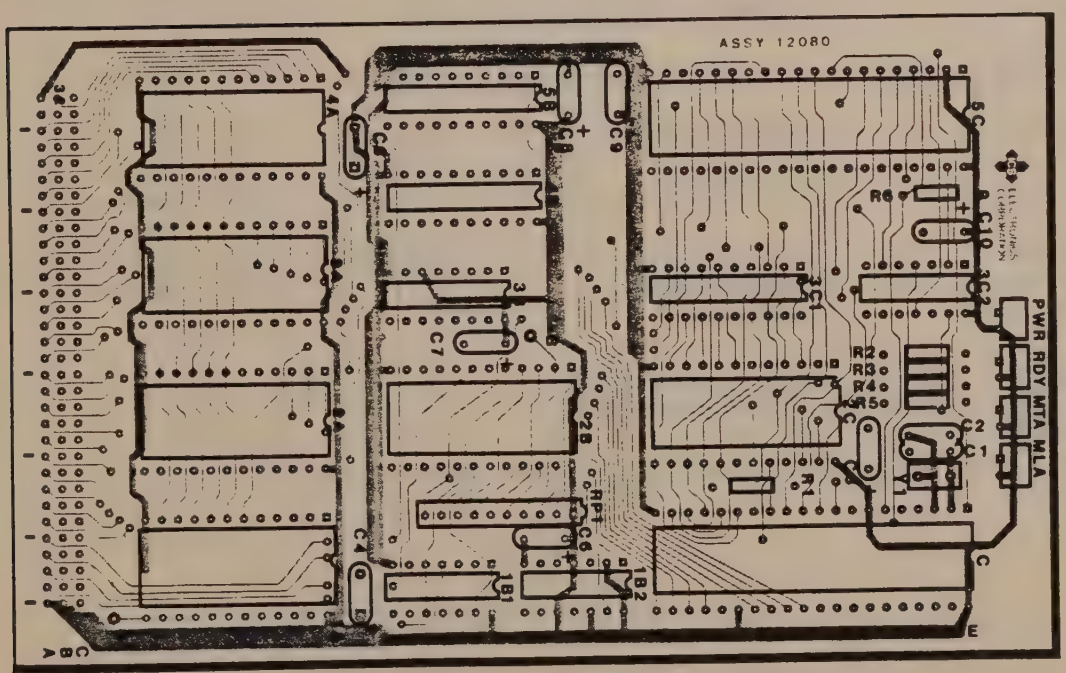


Figure 6-1 4823 Component Layout

TABLE 6-3 4823 PARTS LIST

Stock Number	Qty. Per Assem.	Description	Ref. Desg.	Mfgr.	Mfgr.P/N
112082	01	PCB			
798039	01	IC, CPU, 8039	1C	INL	8039-6
792716	01	IC, PROM, 2716	2C	ICS	-
742373	01	IC, LATCH, 8 BIT	3C1	TI	74LS373
742000	01	IC, QUAD NAND	3C2	TI	74LS00
799914	01	IC, GPIB	5C	TI	TMS9914NL
742086	01	IC, EX OR	1B1	TI	74LS86
742074	01	IC, DUAL D F/F	1B2	TI	74LS74
798243	05	IC, I/O EXPDR	2B,1A,2A 3A,4A	INL	8243
742138	01	IC, DCDR	3B	TI	74LS138
735161	01	IC, BUS XCVR, CTL	4B	TI	75161
735160	01	IC, BUS XCVR, DATA	5B	TI	75160
701003	04	LED, RED, RT ANGLE	CR1-4	DIA	550-0405
903008	02	SOCKET, 40 PIN	(1C)(5C)	AUG	540-AG11D
903007	01	SOCKET, 24 PIN	(2C)	AUG	524-AG11D
606102	01	RESISTOR, 1K, 1/4W, 5%	R1	ABC	RC07GF102J
602161	04	RESISTOR, 160 , 1/4W, 5%	R2-R5	ABC	RC07GF161J
696005	01	RES, SIP, 33K	RP1	BEC	785-1-33K
602333	01	RESISTOR, 33 K, 1/4W, 5%	R6	ABC	RC07GF333J
904003	01	CRYSTAL, 11.0596 MHz		ICS	
524105	01	CAP, TANT, 1.0 uf, 10V	C3	ITT	TAG-F-20-1/10-50
521475	02	CAP, TANT, 4.7 uf, 10V	C4,C5	ITT	TAG-F-20-4.7/10-50
533103	05	CAP, DISK, .01 uf 25V	C6-C10	ERI	5835-000-Y500-1032
548240	02	CAP, MICA, 24 pf	C1,C2	ARC	DM5-240J
902026	01	CONNECTOR, 96 Pin DS		PAN	100-096-453
411204	02	SCREW, 2-56 x 1/2			
431200	02	WASHER, LOCK #2			
420200	02	NUT #2			

7

Drawings, Diagrams, Wire Lists

This section includes the following figures:

7-1 4823 Coupler Module Schematic

7-2 4823 Connector/Switch Board Schematic

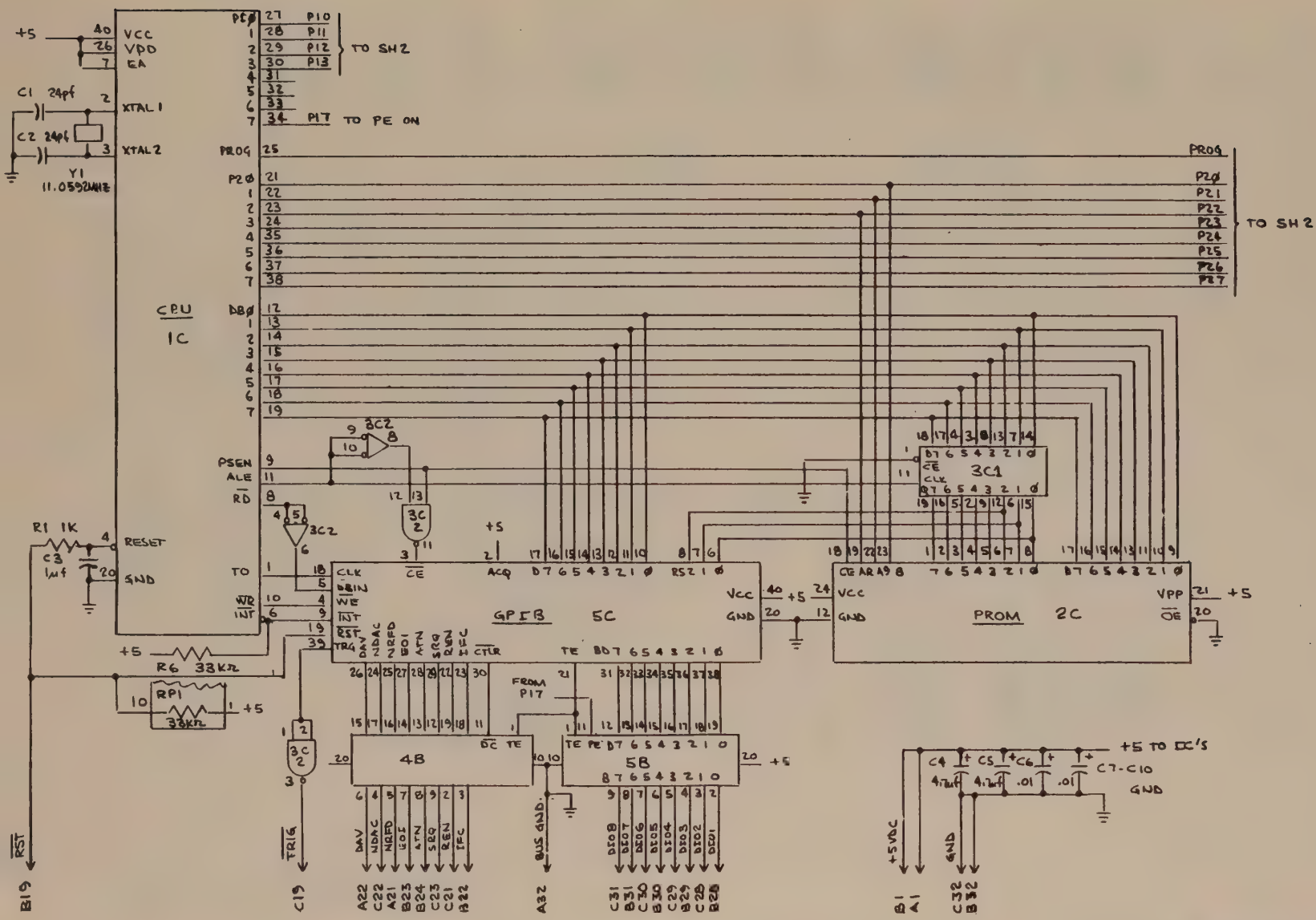
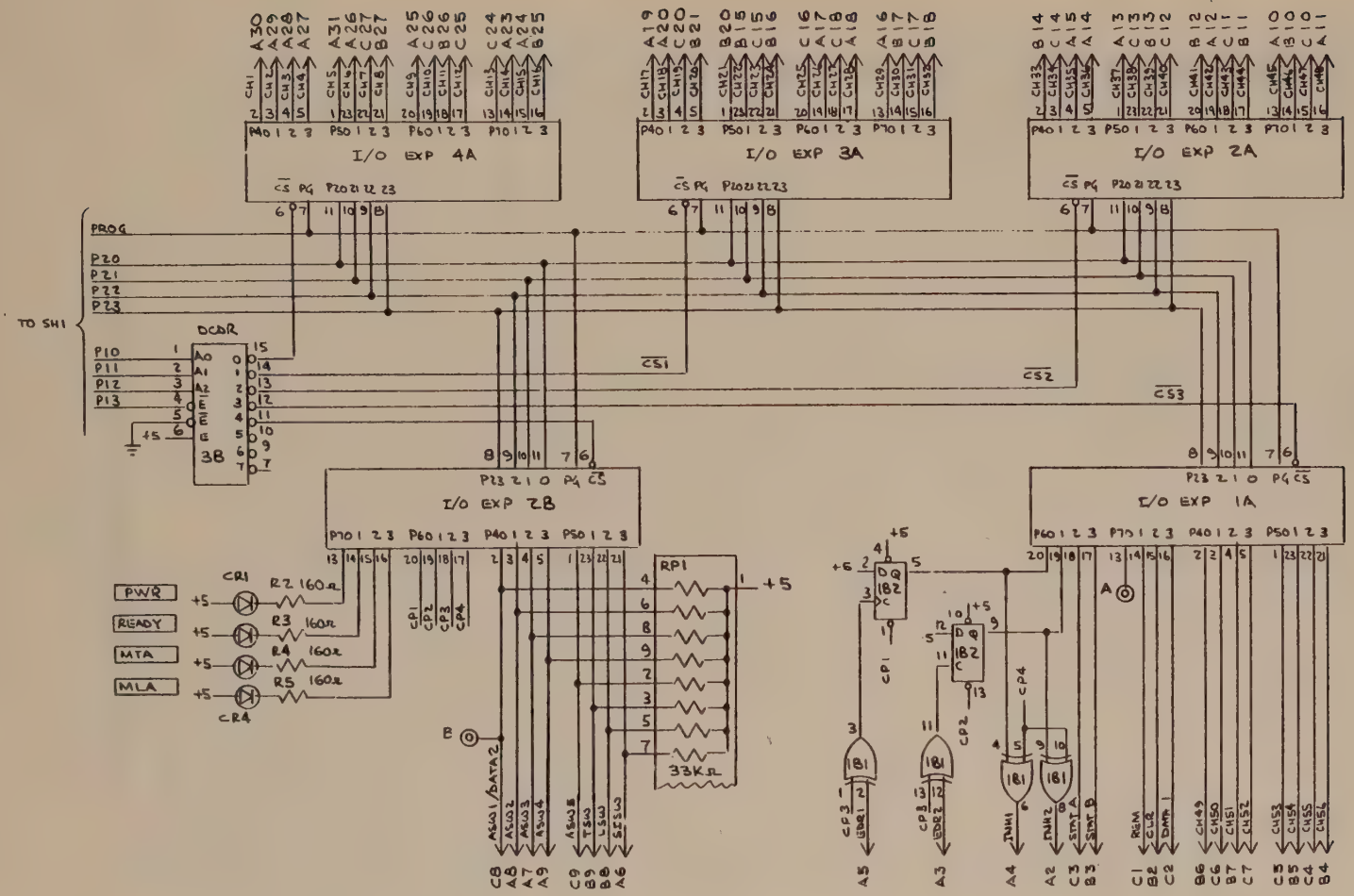


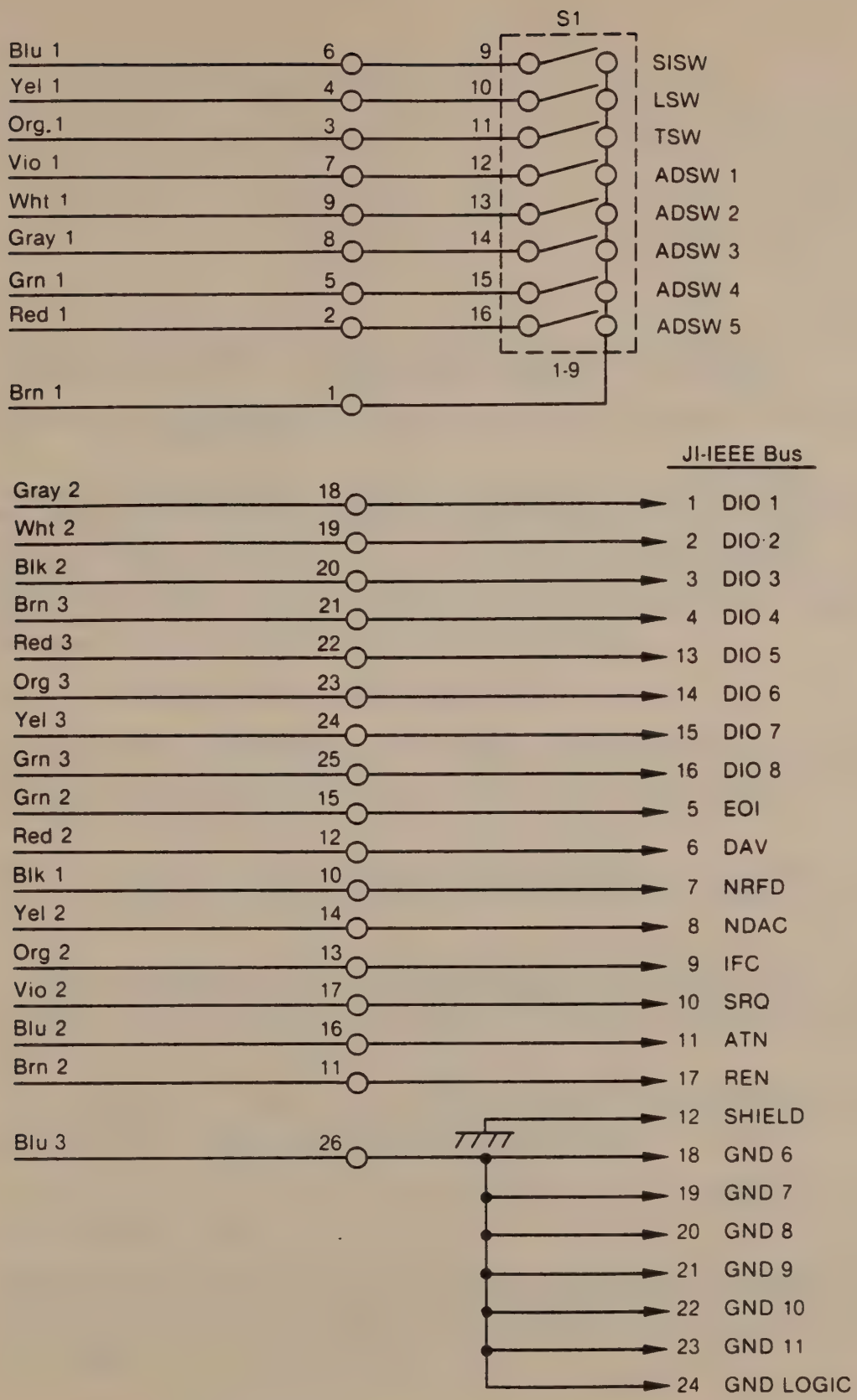
Figure 7-1 Coupler Module Schematic



NOTES

1. ADDRESS SW INPUTS HAVE 32KΩ PULLUPS TO +5V
   ALL OTHER INPUTS NEED EXTERNAL PULLUPS

Figure 7-1 Coupler Module Schematic (continued)



7-2 Connector/Switch Board Schematic

A

4823 PROM Configuration Table

A.1 INTRODUCTION

Appendix A describes the 4823 PROM Configuration Table and provides the user with sufficient information to configure a 4823 Revision 4.0 or later program to meet his interface requirements. The appendix is divided into three parts. The first part provides an overview of the configuration table capabilities. The second part provides a detailed description of each table section. The third part is a listing of the table addresses along with their values for the standard configuration program, F31250, described in Section 1.2.4.

A.2 CONFIGURATION TABLE OVERVIEW

There are twelve configuration tables within the 4823 program. They are located from 300 Hex to 38B Hex. Extreme care must be exercised when modifying these tables. Errors may be of an insidious nature that causes the unit to operate correctly 99% of the time and only foul up rarely!

The Parallel I/O Port Data Configuration Table (PDCT) is used to define each of the 14 four bit I/O ports. Each entry of the PDCT consists of three consecutive bytes of information.

The Serial Poll Response Table (SPRT) contains four eight bit characters which are used as reponses for Serial polls. If a character is used as a Serial Poll response, and that character has the 2^6 bit set to one, then the SRQ line will be set true.

The Configuration of Signal Group (CSG) is used to set the polarity of the various handshake signals. These handshake signals control the flow of data and status information between the 4823 and the host device.

The number of Channels (NOC) entry simply tells the program whether one or two channels are active.

The Talk Format Tables (TFTn) give the exact formats of the Talk channel(s). When the data is transmitted in Talk mode, it is sent exactly as the TFT tables appear (i.e., if a special character is located in the TFT, it is sent as part of the data message).

The Listen Delimiter Tables (LDn) contain input message delimiters. The 4823 will transfer the incoming data to the output ports when it receives a character that is contained within the LD table for the appropriate channel. Listen mode will not be terminated upon receipt of a delimiter, but a data transfer will occur. If the channel is a binary channel, the firmware will not check the LD table until the buffer becomes full. An EOI condition will cause a data transfer at all times for BCD/Hex and binary channels.

The Talk Conversion Tables (TCTn) contains the conversion tables for channels one and two. If a Talk channel is configured as BCD/Hex, the four bit nibbles are converted to eight bit characters by using the appropriate TCT. After conversion, the eight bit character is transmitted onto the Bus. Each TCT contains 16 characters, one for each of the possible Hex digits 0-F.

The BCD/Binary Selector (BBS) indicates the mode of each channel in each direction. Note that each channel and each direction of data transfer is independent. This allows configuration such as channel 1 Listen as binary and channel 1 Talk, channel 2 Talk, and channel 2 Listen as BCD/Hex.

The Listen Word Count (LWC) is simply the number of maximum characters for each Listen channel. The counts will range from 0 to E Hex (14 Decimal) if operating in BCD/Hex mode and 0-7 if Binary.

A.3 DETAIL TABLE DESCRIPTIONS

PARALLEL I/O PORT DATA CONFIGURATION TABLE (PDCT)

BYTE 1:

Bit 7: This bit is set to a 1 if the port is unused. If used, as a Talk or Listen port, this bit is set to a 0. If set to a 1, the program does not examine any other fields in this entry.

Bit 6: If this port is a Talk port, this bit is set to a 1. If the port is a Listen port, it is set to a 0.

Bit 5: If this port is used for channel two, this bit is set to a 1. If this port is used for channel one, this bit is set to a 0.

Bits 0-4: This field of five bits is used to indicate the position in the Listen or Talk message. If it is a Listen port, the count is the number of the "legal" characters in the message prior to this character. It will range from 0 to D Hex (13 Decimal) if BCD/Hex and 0 - 6 if binary. If this is a Talk port, the count is the total number of characters in the appropriate TFT preceeding this character. It will range from 0 - 15 Hex (21 Decimal).

BYTE 2:

Bit 7: If this port is used by a binary channel, this bit is set to a 1. If this port is used by BCD/Hex channel, this bit is set to a 0. If set to a 0, the program will ignore Byte 2, Bit 6.

Bit 6: If this port is used by a binary channel and is the most significant nibble of a binary character, then this bit is set to a 1. Otherwise, this bit is set to a 0.

Bit 5: This bit is unused.

Bit 4: This bit is unused.

Bits 0-3: These bits are set to 1 if the corresponding bits in the I/O port are negative true. For example, if you want all four bits transferred to/from the port as is, these four bits will all be set to 0's. If you want one or more bits to be complemented prior to transfer, set the appropriate bit(s) equal to 1.

BYTE 3:

Bits 4-7: These bits are unused.

Bits 0-3: These bits are set to the actual value (high or low) that you want the corresponding bit in the I/O port set to at PON/reset/IFC/ect time. For example, if all four bits are set to 0's, the I/O port will be set to all 0's at reset time.

SERIAL POLL RESPONSE TABLE (SPRT)

BYTE 1: This eight bit byte is transmitted on the Bus in response to a Serial Poll if neither External Data (EDR) is set true.

BYTE 2: This eight bit byte is transmitted on the Bus if only EDR1 is set true (or EDR1 is set true and channel two is not supported).

BYTE 3: This eight bit type is transmitted on the Bus if channel two is supported and EDR2 is set true and EDR1 is set false.

BYTE 4: This eight bit byte is transmitted on the Bus if channel two is supported and both EDR's are set true.

CONFIGURATION OF SIGNAL GROUP (CSG)

BYTE 1:

Bit 7: This bit is set to the inactive level of Data Strobe 1.

Bit 6: This bit is set to the inactive level of the Clear Strobe.

Bit 5: This bit is set to the Remote level of the Remote/ Local signal.

Bit 4: This bit is set to the inactive level of Data Strobe 2.

Bit 3: This bit is set to the inactive level of Data Inhibit 1 and 2.

Bit 2: This bit is set to the inactive level of External Data Ready 1 and 2.

Bit 1: This bit is set to the ready level of Status B.

Bit 0: This bit is set to the ready level of Status A.

NUMBER OF CHANNELS (NOC)

BYTE 1: This eight bit byte is set to 00 if only one channel is to be supported. If two channels are to be supported, then this byte is set to 80 Hex (128 Decimal).

TALK FORMAT TABLES (TFTn)

TFT1 and TFT2 are both 22 bytes long. They are used to format the Talk messages. After the data characters are assembled, they are inserted into the Talk message as outlined in the appropriate TFT. Each position in the TFT that contains an 80 Hex (128 Decimal) is replaced by a data character converted by a TCT from the appropriate BCD/HEX port. Each position in the TFT that contains an 81 Hex (129 Decimal) is replaced by a data character formed from the two appropriately configured binary ports. The end of the TFT is indicated by a 19 Hex (25 Decimal). The 19 character is not transmitted onto the Bus and all remaining characters are ignored. All other characters (other than a 19 or an 80) in the TFT are transmitted on the Bus as is and are normally stored in the TFT tables as ASCII characters (00 to 7F Hex).

LISTEN DELIMITERS (LDn)

LD1 and LD2 are both six bytes in length. Each byte is a single table entry. Entries are placed into each table starting at the end of the table and working backwards to the beginning of the table. When in Listen mode, the program compares each received character against each entry in the appropriate table. If a match is found, the previously received data is transferred to the output ports and a Data Strobe is issued. Only the least significant 7 bits are relevant in the match attempts. If a table entry is encountered that has the most significant bit set (80-FF Hex), the table search is terminated for that received data character.

TALK CONVERSION TABLES (TCTn)

TCT1 and TCT2 are both 16 bytes in length. These tables are only used for BCD/Hex Talk channels. Each BCD/Hex character, after being read from an I/O port, is translated into an eight bit character. The translation is performed by indexing into the appropriate TCT. For example, a BCD/Hex character of 8 would be replaced by the 9th TCT entry (BCD/Hex 0 would yield entry number 1). Note that the TCT is accessed after the BCD/Hex character is set to the correct polarity.

BCD/BINARY SELECTOR (BBS)

BYTE 1:

Bits 4-7: These bits are unused.

Bit 3: If Talk Channel 2 is binary, then this bit is set to a 1. If Talk Channel 2 is BCD/Hex, then this bit is set to a 0. If channel 2 is not supported, this bit is ignored by the program.

Bit 2: If Talk Channel 1 is binary, then this bit is set to a 1. If Talk Channel 1 is BCD/Hex, then this bit is set to a 0.

Bit 1: If Listen Channel 2 is binary, then this bit is set to a 1. If Listen Channel 2 is BCD/Hex, then this bit is set to a 0. If channel 2 is not supported, then this bit is ignored by the program.

Bit 0: If Listen Channel 1 is binary, then this bit is set to a 1. If Listen Channel 1 is BCD/Hex, then this bit is set to a 0.

LISTEN WORK COUNT (LWC)

BYTE 1:

Bits 4-7: This field of four bits contains a Hex digit which is equal to the maximum number of data characters that will be received from the Bus for channel 2. This Hex digit will range from O to E Hex (14 Decimal) if Listen Channel 2 is BCD/Hex. If Listen Channel 2 is binary, then it will range from 0 to 7. The count is made of only the data characters, not special characters that will not be transferred.

Bits 0-3: This field of four bits contains a Hex digit which is equal to the maximum number of data characters that will be received from the Bus for Channel 1. This Hex digit will range from O to E Hex (14 Decimal) if Listen Channel 1 is BCD/Hex. If Listen Channel 1 is binary, then it will range from 0 to 7. The count is made of only the data characters, not special characters that will not be transferred.

A.4 CONFIGURATION TABLE LISTING

Refer to computer listings on the following pages.

CONFIGURATION TABLE

```
                ;*****************************************
                ; PARALLEL DATA I/O CONFIGURATION TABLE*
                ;   BYTE 1:                            *
                ;    BIT 7= 1 IF PORT IS UNUSED        *
                ;    BIT 6= 1 IF PORT IS A 'TALK' PORT *
                ;    BIT 5= 1 IF PORT IS FOR CHANNEL 2 *
                ;                                      *
                ;    BIT 4= CHARACTER NUMBER:          *
                ;    BIT 3  -TALK: CHAR POS # IN       *
                ;    BIT 2   FORMAT TABLE.             *
                ;    BIT 1  -LISTEN: N'TH LEGAL CHAR.  *
                ;    BIT 0  -RANGE- FROM 0-1FH.        *
                ;                                      *
                ;   BYTE 2:                            *
                ;    BIT 7= 1 PORT IS 1/2 BINARY CHAR  *
                ;    BIT 6= 1 PORT IS MOST SIG. NIBBLE *
                ;           OF A BINARY CHARACTER      *
                ;    BIT 5= UNUSED                     *
                ;    BIT 4= UNUSED                     *
                ;                                      *
                ;    BIT 3= 1 IF PORT BIT 3 IS NEG TRUE*
                ;    BIT 2= 1 IF PORT BIT 2 IS NEG TRUE*
                ;    BIT 1= 1 IF PORT BIT 1 IS NEG TRUE*
                ;    BIT 0= 1 IF PORT BIT 0 IS NEG TRUE*
                ;                                      *
                ;   BYTE 3:                            *
                ;    BIT 7= UNUSED                     *
                ;    BIT 6=   "                        *
                ;    BIT 5=   "                        *
                ;    BIT 4=   "                        *
                ;                                      *
                ;    BIT 3= PORT BIT 3 RESET LEVEL     *
                ;    BIT 2= PORT BIT 2 RESET LEVEL     *
                ;    BIT 1= PORT BIT 1 RESET LEVEL     *
                ;    BIT 0= PORT BIT 0 RESET LEVEL     *
                ;                                      *
                ;  BYTE:     #1         #2         #3   *
                ;  BIT:  -76543210--76543210--76543210- *
0300 00         PDCT DB   00000000B,00000000B,00000000B *
0303 01              DB   00000001B,00000000B,00000000B *
0306 02              DB   00000010B,00000000B,00000000B *
0309 03              DB   00000011B,00000000B,00000000B *
030C 04              DB   00000100B,00000000B,00000000B *
030F 05              DB   00000101B,00000000B,00000000B *
0312 06              DB   00000110B,00000000B,00000000B *
0315 40              DB   01000000B,00000000B,00000000B *
0318 41              DB   01000001B,00000000B,00000000B *
031B 42              DB   01000010B,00000000B,00000000B *
031E 43              DB   01000011B,00000000B,00000000B *
0321 44              DB   01000100B,00000000B,00000000B *
0324 45              DB   01000101B,00000000B,00000000B *
0327 46              DB   01000110B,00000000B,00000000B *
                ;*****************************************
```

```
ICS ELECT.  8048 RDOS MACRO-ASSEMBLER

                ****************************************
                * SERIAL POLL RESPONSE TABLE           *
                *   THESE 4 CHAR'S ARE USED AS THE RE- *
                *   SPONSES FOR THE SPECIFIED CONDITION*
                *                                      *
                *  LIST OF CHAR'S OUTPUT IF:           *
032A 00         SPRT    DB    00H       NO EDR IS SET   *
032B 41                 DB    41H       EDR1 IS SET     *
032C 00                 DB    00H       EDR2 IS SET     *
032D 00                 DB    00H       BOTH EDR'S ARE SET*
                ****************************************



                ****************************************
                * CONFIGURATION OF HANDSHAKE SIGNALS   *
                *                                      *
                *   BIT 7 = DATA STB1 INACTIVE STATE   *
                *   BIT 6 = CLR STB INACTIVE STATE     *
                *   BIT 5 = REM/LOC (REMOTE STATE)     *
                *   BIT 4 = DATA STB2 INACTIVE STATE   *
                *   BIT 3 = /INH STATE                 *
                *   BIT 2 = /EDR STATE                 *
                *   BIT 1 = CHAN 2 READY STATE         *
                *   BIT 0 = CHAN 1 READY STATE         *
                *                                      *
                *          -76543210-                  *
032E 49         CSG     DB   01001001B                 *
                ****************************************



                ****************************************
                * NUMBER OF CHANNELS                   *
                *                                      *
                *   00H = IF ONE CHANNEL               *
                *   80H = IF TWO CHANNELS              *
                *                                      *
032F 00         NOC     DB   00H                       *
                ****************************************
```

CONFIGURATION TABLE (Continued)

```
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                        ****************************************
                        * TALK FORMAT TABLES 1 AND 2           *
                        *    80H = DATA CHAR(BCD)              *
                        *    81H = DATA CHAR(BIN)              *
                        *    19H = END-OF-MESSAGE (EOM)        *
                        *    XXH = DATA SENT AS IS             *
                        * NOTE: THE EOM CHAR ISN'T SENT.       *
                        *                                      *
                        * CHANNEL 1 TABLE                      *
0330 80                 TFT1    DB    80H       CH1 CHAR  1     *
0331 80                         DB    80H        "     "  2     *
0332 80                         DB    80H        "     "  3     *
0333 80                         DB    80H        "     "  4     *
0334 80                         DB    80H        "     "  5     *
0335 80                         DB    80H        "     "  6     *
0336 80                         DB    80H        "     "  7     *
0337 0D                         DB    0DH       CR              *
0338 0A                         DB    0AH       LF              *
0339 19                         DB    19H       END-OF-MSG CHAR *
033A 00                         DB    0         NOT USED        *
033B 00                         DB    0          "    "         *
033C 00                         DB    0          "    "         *
033D 00                         DB    0          "    "         *
033E 00                         DB    0          "    "         *
033F 00                         DB    0          "    "         *
0340 00                         DB    0          "    "         *
0341 00                         DB    0          "    "         *
0342 00                         DB    0          "    "         *
0343 00                         DB    0          "    "         *
0344 00                         DB    0          "    "         *
0345 00                         DB    0          "    "         *
0346 19                         DB    19H       PERM EOM CHAR!!! *
                        *                                      *
                        * CHANNEL 2 TABLE                      *
0347 19                 TFT2    DB    19H       NOT USED        *
0348 00                         DB    0          "    "         *
0349 00                         DB    0          "    "         *
034A 00                         DB    0          "    "         *
034B 00                         DB    0          "    "         *
034C 00                         DB    0          "    "         *
034D 00                         DB    0          "    "         *
034E 00                         DB    0          "    "         *
034F 00                         DB    0          "    "         *
0350 00                         DB    0          "    "         *
0351 00                         DB    0          "    "         *
0352 00                         DB    0          "    "         *
0353 00                         DB    0          "    "         *
```

```
0354 00                 DB    0             "    "                *
0355 00                 DB    0             "    "                *
0356 00                 DB    0             "    "                *
0357 00                 DB    0             "    "                *
0358 00                 DB    0             "    "                *
0359 00                 DB    0             "    "                *
035A 00                 DB    0             "    "                *
035B 00                 DB    0             "    "                *
035C 00                 DB    0             "    "                *
035D 19                 DB    19H           PERM EOM CHAR!!!       *

                        ****************************************
                        * LISTEN DELIMITORS FOR CH1 AND CH2      *
                        *   80H = ENTRY POS. NOT USED            *
                        *   00H-7FH = DELIMITOR                  *
                        * NOTE: START FROM THE END OF EACH TABLE *
                        *       AS THAT SPEEDS UP THE PROGRAM    *
                        *                                        *
                        * CHANNEL 1 TABLE                        *
035E 80                 LD1   DB    80H           DELIM 6  (UNUSED)*
035F 80                       DB    80H                 5  (UNUSED)*
0360 80                       DB    80H                 4  (UNUSED)*
0361 2C                       DB    2CH                 3  (COMMA) *
0362 0A                       DB    0AH                 2  (LF)    *
0363 0D                       DB    0DH                 1  (CR)    *
                        *                                        *
                        * CHANNEL 2 TABLE                        *
0364 80                 LD2   DB    80H           DELIM 6  (UNUSED)*
0365 80                       DB    80H                 5  (UNUSED)*
0366 80                       DB    80H                 4  (UNUSED)*
0367 80                       DB    80H                 3  (UNUSED)*
0368 80                       DB    80H                 2  (UNUSED)*
0369 80                       DB    80H                 1  (UNUSED)*
                        ****************************************

                        ****************************************
                        * TALK CONVERSION TABLE FOR CH1 AND CH2*
                        *   IF BCD/HEX, THESE EIGHT BIT CHAR'S *
                        *   ARE SUBSTITUTED FOR THE HEX DIGITS *
                        *   0 THROUGH F (15 DECIMAL).          *
                        *                                      *
                        * CHANNEL 1 TABLE                      *
                        *           -0123456789ABCDEF-         *
036A 30                 TCT1  DB    '0123456789+- ,E '         *
                        *                                      *
                        * CHANNEL 2 TABLE                      *
                        *           -0123456789ABCDEF-         *
037A 2D                 TCT2  DB    '----(UNUSED)----'         *
                        ****************************************
```

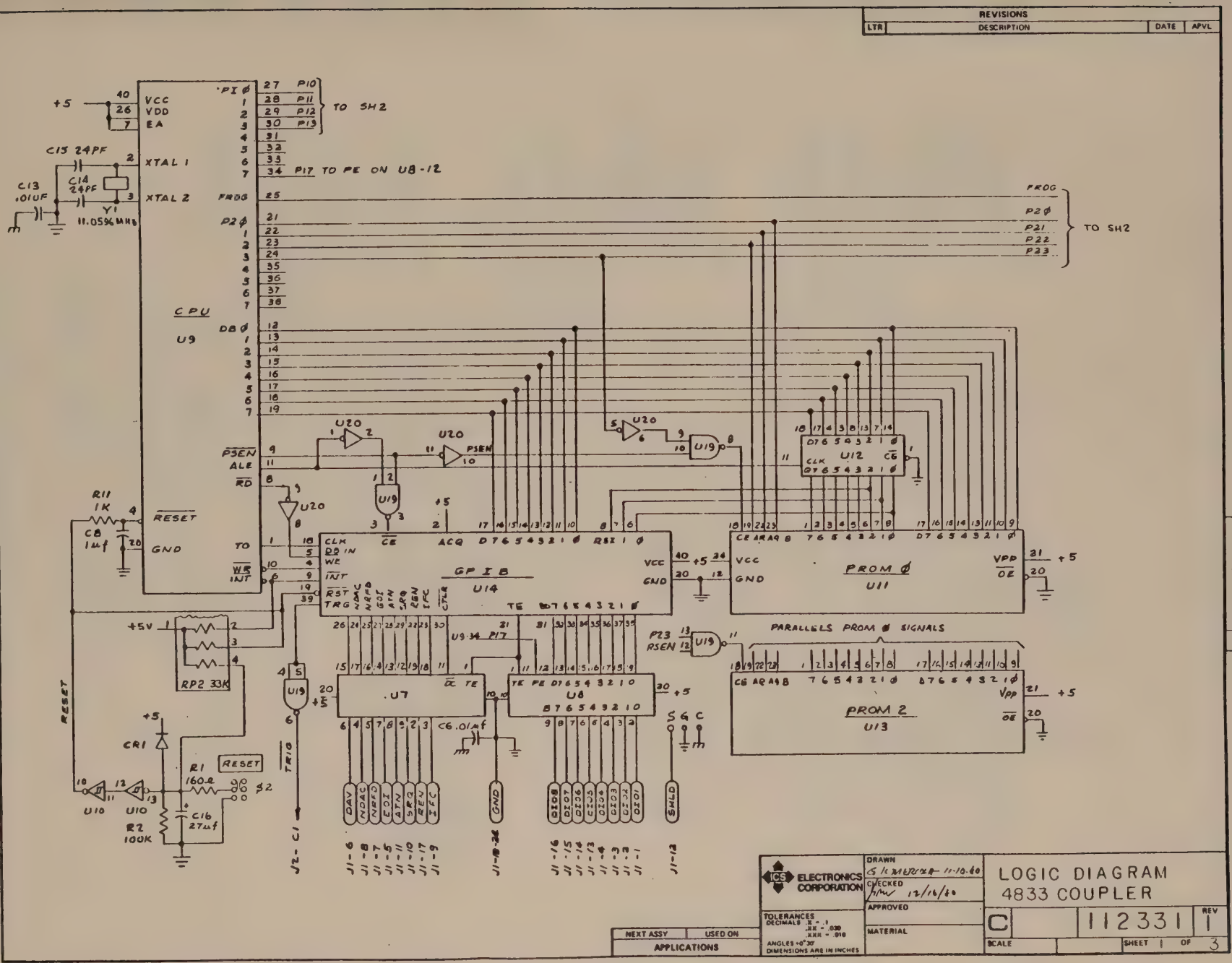
```
ICS ELECT.  8048 RDOS MACRO-ASSEMBLER

                        ;*****************************************
                        ; BCD/BINARY SELECTOR                     *
                        ;  BIT 7 = UNUSED                        *
                        ;  BIT 6 = UNUSED                        *
                        ;  BIT 5 = UNUSED                        *
                        ;  BIT 4 = UNUSED                        *
                        ;                                        *
                        ;  BIT 3 = 1 IF CH2 IS A BINARY TALKER  *
                        ;  BIT 2 = 1 IF CH1 IS A BINARY TALKER  *
                        ;  BIT 1 = 1 IF CH2 IS A BINARY LISTENER
                        ;  BIT 0 = 1 IF CH1 IS A BINARY LISTENER
                        ;                                       *
                        ; CORRESPONDING BIT MUST BE SET IF ANY  *
                        ;  - REPEAT - ANY PORT IS BINARY        *
                        ;                                       *
                        ;           -76543210-                  *
038A 00                 BBS     DB   00000000B                  *
                        ;*****************************************

                        ;*****************************************
                        ; LISTEN WORD COUNT                      *
                        ;  NUMBER OF LEGAL DATA CHAR'S FROM BUS*
                        ;    MOST SIG 4 BITS = CHANNEL 2 COUNT *
                        ;    LEAST SIG 4 BITS = CHANNEL 1 COUNT*
                        ;                                       *
038B 07                 LWC     DB   07H                        *
                        ;*****************************************

ICS ELECT.  8048 RDOS MACRO-ASSEMBLER

                        END
```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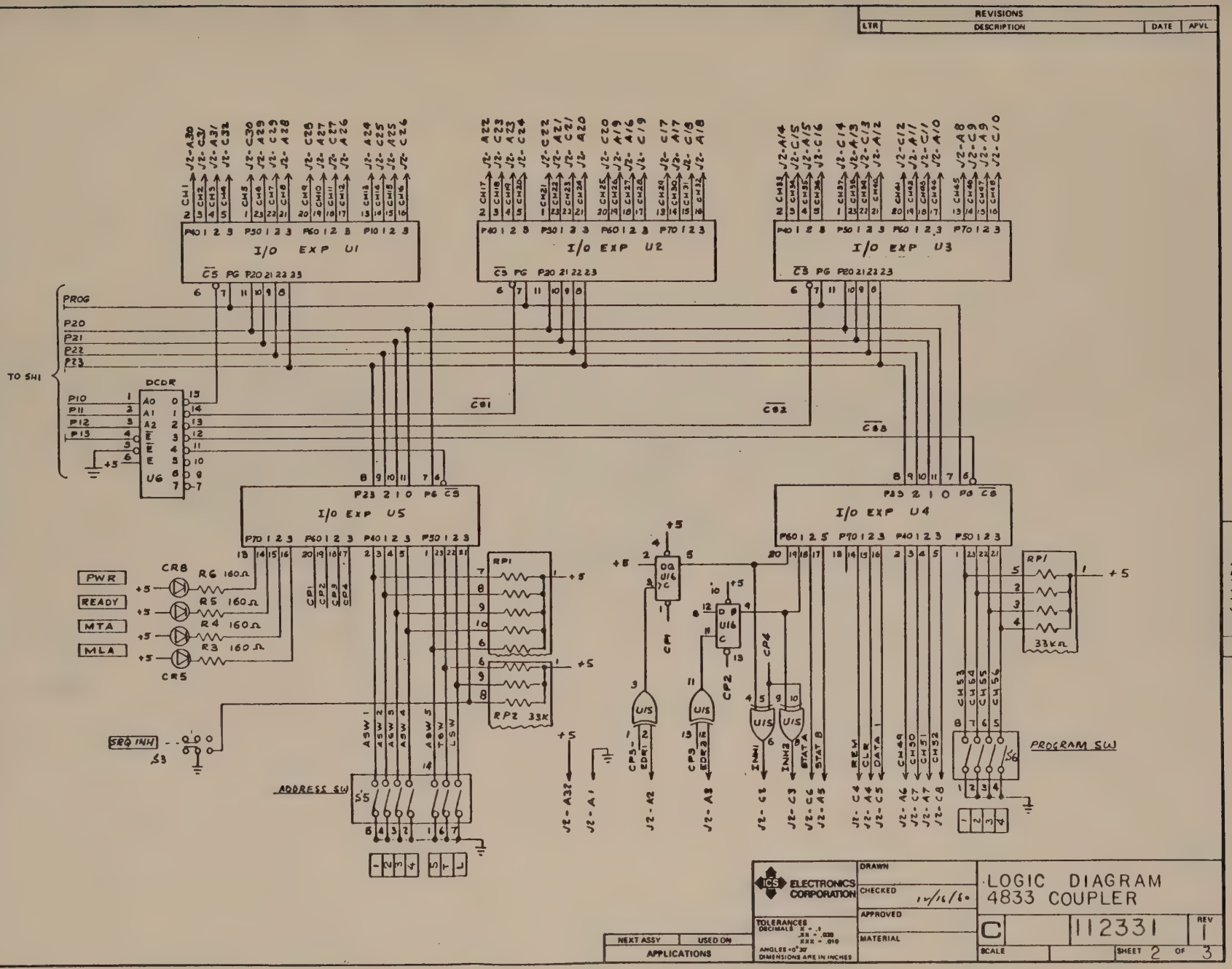
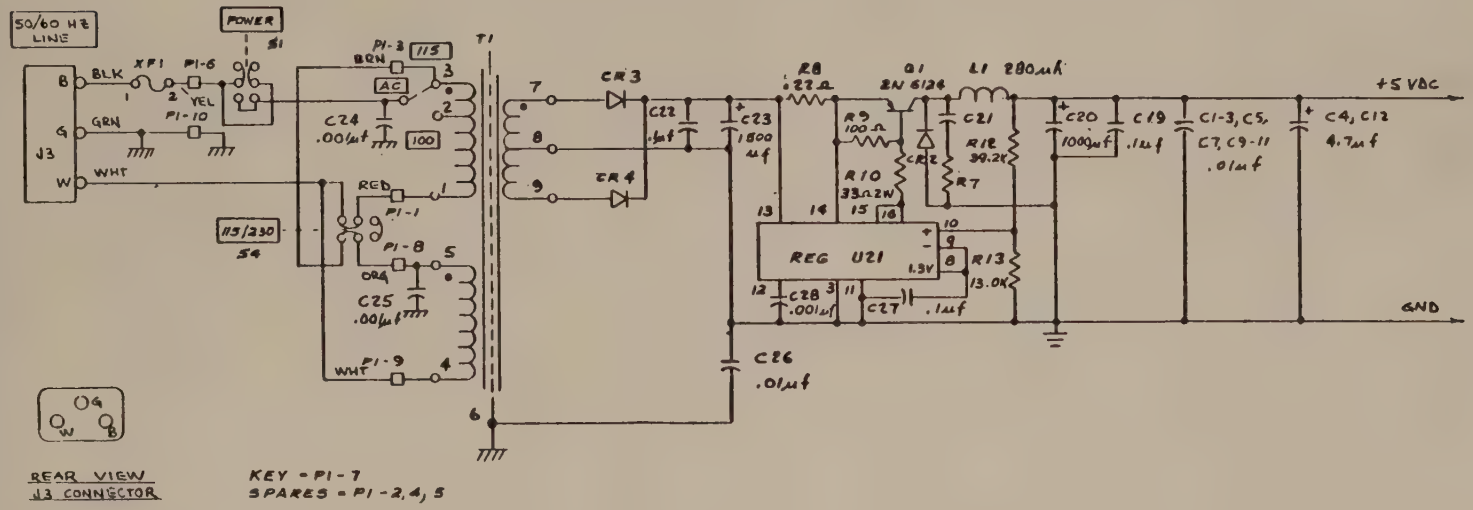
LTR
DESCRIPTION
DATE
APVL
CPU
U9
VCC
VDD
EA
XTAL 1
XTAL 2
RESET
GND
PSEN
ALE
RD
WR
INT
TO
PROG
P10
P11
P12
P13
P17 TO PE ON U8-12
TO SH2
C13 24PF
C14 24PF
C13 .01UF
Y1 11.0596 MHz
R11 1K
CB 1uf
RP2 33K
CR1
R1 160Ω
R2 100K
C16 27uf
C6 .01uf
S2
RESET
TRIG
J2-C1
U10
U19
U20
U7
U8
U11
U12
U13
GPIB
U14
PROM Ø
PROM 2
PARALLELS PROM Ø SIGNALS
DAV
NDAC
NRFD
EOI
ATN
SRQ
REN
IFC
GND
SHLD
J1-6
J1-7
J1-8
J1-17
J1-5
J1-10
J1-11
J1-9
J1-16
J1-15
J1-14
J1-13
J1-4
J1-3
J1-2
J1-1
J1-12
J1-18,24
ICS ELECTRONICS CORPORATION
DRAWN
CHECKED
APPROVED
MATERIAL
TOLERANCES
DECIMALS .X = .1
.XX = .030
.XXX = .010
ANGLES ±0°30'
DIMENSIONS ARE IN INCHES
NEXT ASSY
USED ON
APPLICATIONS
LOGIC DIAGRAM
4833 COUPLER
C
112331
REV
1
SCALE
SHEET 1 OF 3
112331


REVISIONS
LTR
DESCRIPTION
DATE
APVL
I/O EXP U1
I/O EXP U2
I/O EXP U3
I/O EXP U5
I/O EXP U4
DCDR
U6
PROG
P20
P21
P22
P23
TO SHI
PWR
READY
MTA
MLA
CR8
CR5
R6 160Ω
R5 160Ω
R4 160Ω
R3 160Ω
RP1
RP2 33K
33KΩ
SRQ INH
S3
ADDRESS SW
S5
PROGRAM SW
S6
ASW 1
ASW 2
ASW 3
ASW 4
ASW 5
TSW
LSW
INH1
INH2
STAT A
STAT B
REM
CLR
DATA I
CP1
CP2
CP3
CP4
EDR 1
EDR 2
U15
U16
+5
ELECTRONICS CORPORATION
DRAWN
CHECKED
10/16/80
APPROVED
MATERIAL
TOLERANCES
DECIMALS X ± .1
XX ± .030
XXX ± .010
ANGLES ±0°30'
DIMENSIONS ARE IN INCHES
NEXT ASSY
USED ON
APPLICATIONS
LOGIC DIAGRAM
4833 COUPLER
C
112331
REV
1
SCALE
SHEET 2 OF 3

REVISIONS			
LTR	DESCRIPTION	DATE	APVL



REAR VIEW
J3 CONNECTOR

KEY = P1-7
SPARES = P1-2, 4, 5

NEXT ASSY	USED ON
APPLICATIONS	

ELECTRONICS CORPORATION

DRAWN

CHECKED 12/16/70

APPROVED

MATERIAL

TOLERANCES
DECIMALS X = .1
.XX = .030
.XXX = .010
ANGLES ±0°30'
DIMENSIONS ARE IN INCHES

LOGIC DIAGRAM
4833 COUPLER

C | 112331 | REV 1

SCALE

SHEET 3 OF 3

112331

WARRANTY

ITHACO Inc. warrants each instrument to be free of defects in material and workmanship for a period of one year after shipment to the original purchaser; batteries are specifically excluded. Liability under this warranty is limited to repairing or adjusting any instrument returned to the factory for that purpose. The warranty of this instrument is void if the instrument has been modified other than in accordance with written instructions from ITHACO, or if defect or failure is judged by ITHACO to be caused by abnormal conditions of operation, storage or transportation.

This warranty is subject to verification by ITHACO, that a defect or failure exists, and to compliance by the original purchaser with the following instructions:

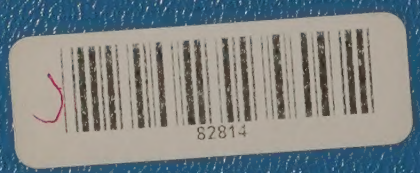
1. Before returning the instrument, notify ITHACO with full details of the problem; include model number and serial number of the instrument involved.

2. After receiving the above information, ITHACO will give you shipping instructions or service instructions. After receipt of shipping instructions, ship the instrument to ITHACO. Full liability for damage during shipment is borne by the purchaser. It is recommended that instruments shipped to us be fully insured and packed surrounded by at least 2 inches of shock-absorbing material.

ITHACO reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This warranty is expressly in lieu of all other obligations or liabilities on the part of ITHACO, and ITHACO neither assumes, nor authorizes any other person to assume for it, any liability in connection with the sales of ITHACO instruments.

ITHACO INC.
735 W. Clinton Street
Ithaca, New York 14850
Telephone: 607-272-7640


82814